

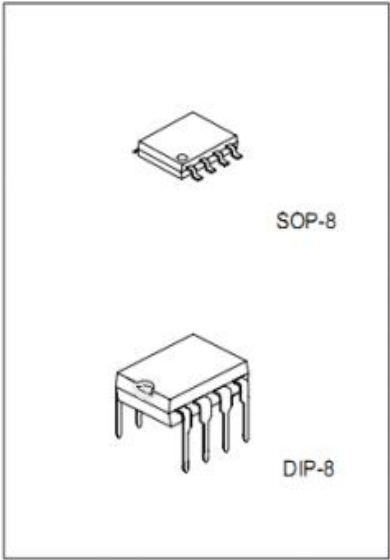
SINGLE TIMER

DESCRIPTION

The LC NE555 is a highly stable timer integrated circuit. It can be operated in both Astable and Monostable mode. With monostable operation, the time delay is precisely controlled by one external and one capacitor. With a stable operation as an oscillator the frequency and duty cycle are both accurately controlled with two external resistors and one capacitor.

FEATURES

- *High current driver capability(=200mA).
- *Adjustable duty cycle.
- *Timing from μs to hours.
- *Turn off time less than $2\mu s$.
- *Operates in both astable and monostable modes.



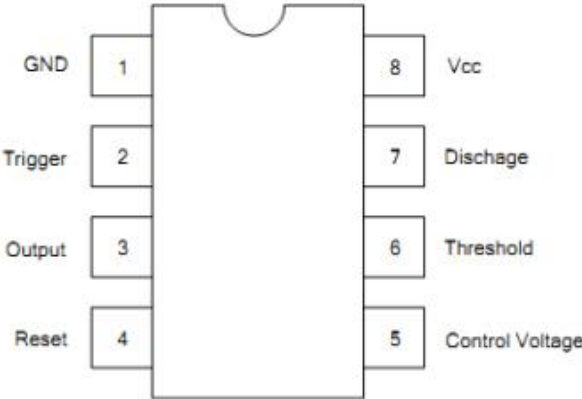
*Pb-free plating product number: NE555L

ORDERING INFORMATION

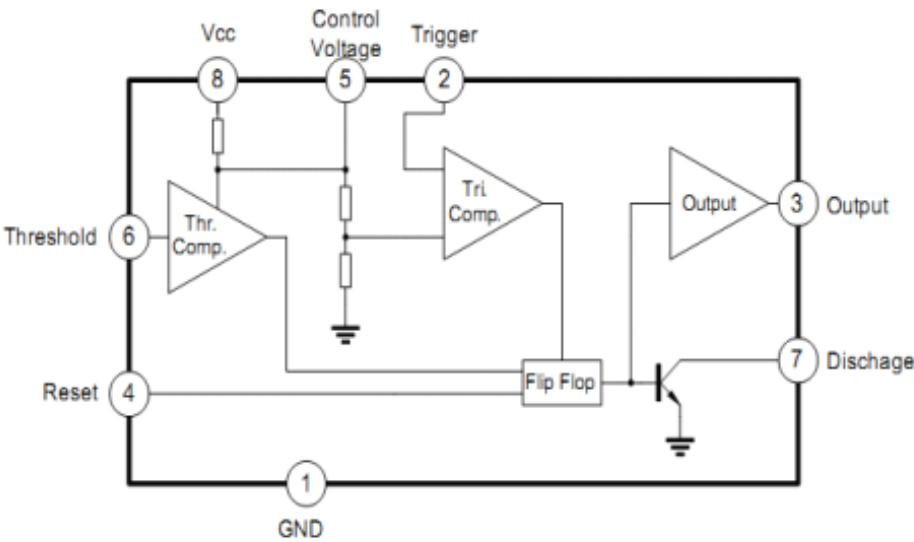
Ordering Number		Package	Packing
Normal	Lead Free Plating		
NE555-D08-T	NE555L-D08-T	DIP-8	Tube
NE555-S08-R	NE555L-S08-R	SOP-8	Tape Reel
NE555-S08-T	NE555L-S08-T	SOP-8	Tube

NE555L-D08-T	(1)Packing Type	(1) R: Tape Reel T: Tube
	(2)Package Type	(2) D08: DIP-8, S08: SOP-8
	(3)Lead Plating	(3) L: Lead Free Plating Blank: Pb/Sn

PIN CONFIGURATION



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	16	V
Power Dissipation	P_D	600	mW
Junction Temperature	T_J	+125	°C
Operating Temperature	T_{OPR}	-20 ~ +85	°C
Storage Temperature	T_{STG}	-40 ~ +150	°C

Note:1.Absolute maximum ratings and operation rating recommended are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2.The device is guaranteed to meet performance specification within 0°C~+70°C operating temperature range and assured by design from -20°C~+85°C.

■ **ELECTRICAL CHARACTERISTICS** ($V_{CC}=5 \sim 15V$, $T_a=25^{\circ}C$, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		4.5		16	V
Supply Current (Note 1)	I_{CC}	$V_{CC}=5V$, $R_L=\infty$		3	6	mA
		$V_{CC}=15V$, $R_L=\infty$		7.5	15	mA
Initial Accuracy (Note 2)	Monostable	A_{CURR}	$R_A=1k \sim 100k\Omega$	1.0	3.0	%
	Astable			2.25		%
Drift with Temperature	Monostable	$\Delta t/\Delta T$	$C=0.1\mu F$	50		ppm/ $^{\circ}C$
	Astable			150		ppm/ $^{\circ}C$
Drift with Supply Voltage	Monostable	$\Delta t/\Delta V_{CC}$		0.1	0.5	%/V
	Astable			0.3		%/V
Control Voltage	V_C	$V_{CC}=15V$	9.0	10.0	11.0	V
		$V_{CC}=5V$	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	$V_{CC}=15V$		10.0		V
		$V_{CC}=5V$		3.33		V
Threshold Current(Note 3)	I_{TH}			0.1	0.25	μA
Trigger Voltage	V_{TR}	$V_{CC}=5V$	1.1	1.67	2.2	V
		$V_{CC}=15V$	4.5	5	5.6	V
Trigger Current	I_{TR}	$V_{TR}=0$		0.01	2.0	μA
Reset Voltage	V_{RST}		0.4	0.7	1.0	V
Reset Current	I_{RST}			0.1	0.4	mA
Low Output Voltage	V_{OL}	$V_{CC}=15V$				
		$I_{SINK}=10mA$		0.06	0.25	V
		$I_{SINK}=50mA$		0.3	0.75	V
		$V_{CC}=5V$				
High Output Voltage	V_{OH}	$I_{SINK}=5mA$		0.05	0.35	V
		$V_{CC}=15V$				
		$I_{SOURCE}=200mA$		12.5		V
		$I_{SOURCE}=100mA$	12.75	13.3		V
Rise Time of Output	t_R	$V_{CC}=5V$, $I_{SOURCE}=100mA$	2.75	3.3		V
Fall Time of Output	t_F			100		ns
Discharge Leakage Current	I_{LKG}			100		nA

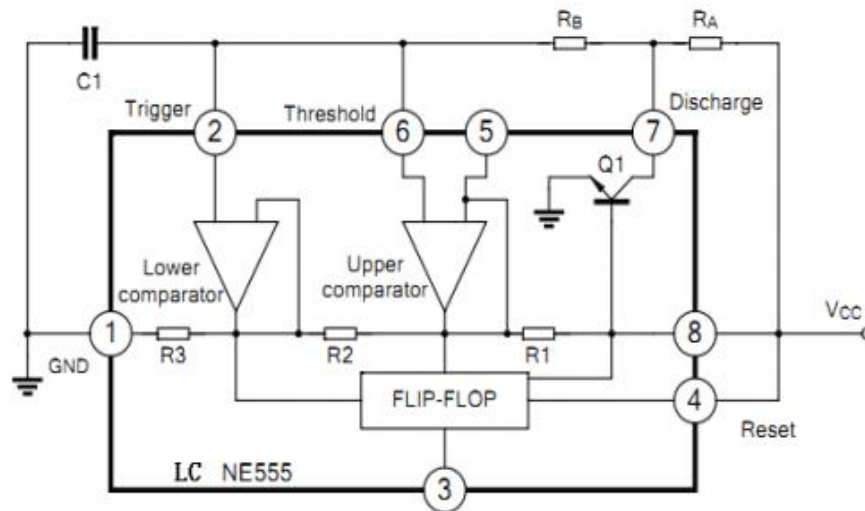
Note 1: Supply current when output high typically 1mA less at $V_{CC}=5V$.

Note 2: Tested at $V_{CC}=5.0V$ and $V_{CC}=15V$.

Note 3: This will determine the maximum value of R_A+R_B for 15V operation, The maximum total is $R=20M\Omega$, and for 5V operation the maximum total is $R=6.7M\Omega$.

NE555

■ TYPICAL APPLICATION CIRCUIT



■ TYPICAL APPLICATION NOTES

The application circuit shows astable mode configuration.

Pin 6 (Threshold) is tied to Pin 2 (Trigger) and Pin 4 (reset) is tied to VCC (Pin 8). The external capacitor C1 of Pin 6 and Pin 2 charges through RA, RB and discharges through RB only. In the internal circuit of UTC NE555, one input of the upper comparator is at voltage of 2/3VCC (R1=R2=R3), another input is connected to Pin 6. As soon as C1 is charging to higher than 2/3VCC, transistor Q1 is turned ON and discharge C1 to collector voltage of transistor Q1. Therefore, the flip-flop circuit is reset and output is low. One input of lower comparator is at voltage of 1/3VCC, discharge transistor Q1 turn off and C1 charges through RA and RB. Therefore, the flip-flop circuit is set output high.

That is, when C1 charges through RA and RB, output is high and when C1 discharge through RB, output is low. The charge time (output is high) t1 is 0.693 (RA+RB) C1 and the discharge time (output is low) T2 is 0.693 RB C1.

$$\ln \left(\frac{V_{CC} - \frac{1}{3}V_{CC}}{V_{CC} - \frac{2}{3}V_{CC}} \right) = 0.693$$

$$T1 = 0.693 (RA + RB) C1$$

$$T2 = 0.693 RB C1$$

Thus the total period time T is given by

$$T = T1 + T2 = 0.693 (RA + 2RB) C1.$$

Then the frequency of astable mode is given by

$$f = \frac{1}{T} = \frac{1.44}{(RA + 2RB) C1}$$

The duty cycle is given by

$$D.C. = \frac{T2}{T} = \frac{RB}{RA + 2RB}$$