## Features

- $V_{DS (V)}$ = 30V
- I_D = 5.3 A
- $R_{DS(ON)} < 50m\Omega$ (V_{GS} = -10V)
- $R_{DS(ON)} < 80m\Omega$ (V_{GS} = -4.5V)
- Generation VTechnology
- Ultra Low On-Resistance
- Surface Mount
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free
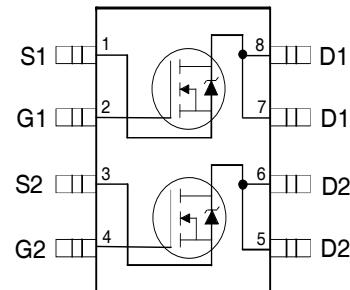
SOP-8

Description

The SOP-8 has been modied through a customizec leadframe for enhanced thermal characteristics and multiple die capability making it ideal in a variety of power applications.

With these improvements. multiple devices can be used in an application with dramatically reduced board space.

The package is designed for vapor phase. intra red. or wave soldering techniques. Power dissipation of gre-ater than 0.8W is possible in a typical PCB mount app-lication.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_A = 25°C	10 Sec. Pulsed Drain Current, V_{GS} @ 10V	5.3	A
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	4.9	
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	3.9	
I_{DM}	Pulsed Drain Current ①	20	
P_D @ T_A = 25°C	Power Dissipation	2.0	W
	Linear Derating Factor	0.016	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	℃

Thermal Resistance Ratings

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient④		62.5	°C/W

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30			V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.032		V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance			50	mΩ	V_{GS} = 10V, I_D = 2.4A ③
				80		V_{GS} = 4.5V, I_D = 2.0A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0			V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	5.2			S	V_{DS} = 15V, I_D = 2.4A
I_{DSS}	Drain-to-Source Leakage Current			1.0	µA	V_{DS} = 24V, V_{GS} = 0V
				25		V_{DS} = 24V, V_{GS} = 0V, T_J = 125 °C
I_{GSS}	Gate-to-Source Forward Leakage			100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage			-100		V_{GS} = - 20V
Q_g	Total Gate Charge			25		I_D = 2.4A
Q_{gs}	Gate-to-Source Charge			2.9	nC	V_{DS} = 24V
Q_{gd}	Gate-to-Drain ("Miller") Charge			7.9		V_{GS} = 10V, See Fig. 6 and 12 ③
$t_{d(on)}$	Turn-On Delay Time		6.8			V_{DD} = 15V
t_r	Rise Time		21		ns	I_D = 2.4A
$t_{d(off)}$	Turn-Off Delay Time		22			R_G = 6.0Ω
t_f	Fall Time		7.7			R_D = 6.2Ω, See Fig. 10 ③
L_D	Internal Drain Inductance		4.0		nH	Between lead tip and center of die contact
L_S	Internal Source Inductance		6.0			
C_{iss}	Input Capacitance		520			V_{GS} = 0V
C_{oss}	Output Capacitance		180		pF	V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance		72			f = 1.0MHz, See
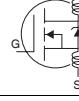
Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)			2.5	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①			20		
V_{SD}	Diode Forward Voltage			1.0	V	T_J = 25°C, I_S = 1.8A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time		47	71	ns	T_J = 25°C, I_F = 2.4A
Q_{rr}	Reverse RecoveryCharge		56	84	nC	di/dt = 100A/µs ③
t_{on}	Forward Turn-On Time		Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)			
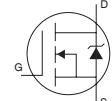
Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② $I_{SD} \leq$ 2.4A, di/dt $\leq$ 73A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C

③ Pulse width $\leq$ 300µs; duty cycle $\leq$ 2%.

④ Surface mounted on FR-4 board, t $\leq$ 10sec.
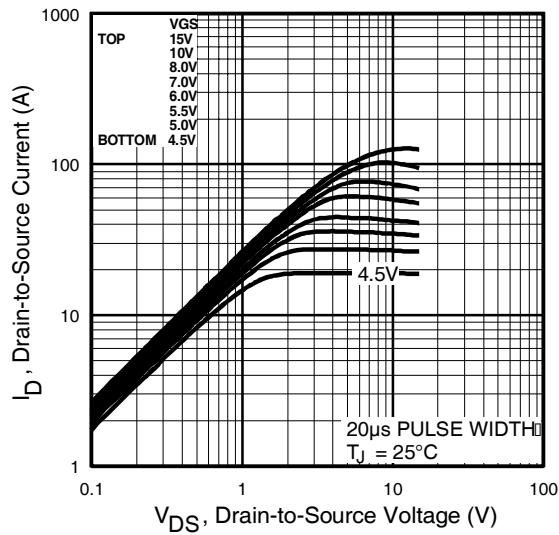
**Fig 1.** Typical Output Characteristics
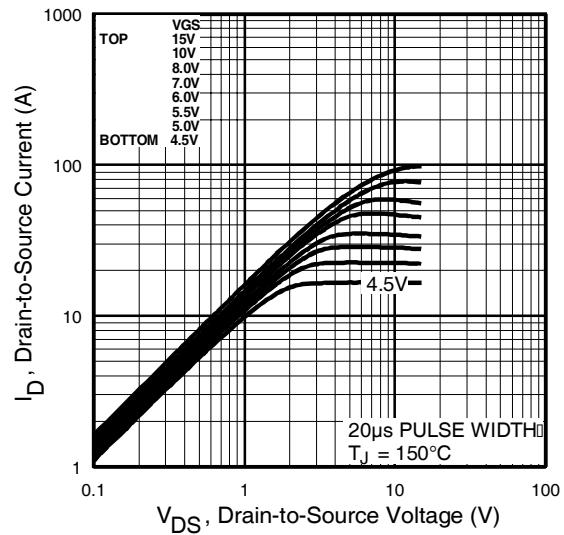
**Fig 2.** Typical Output Characteristics
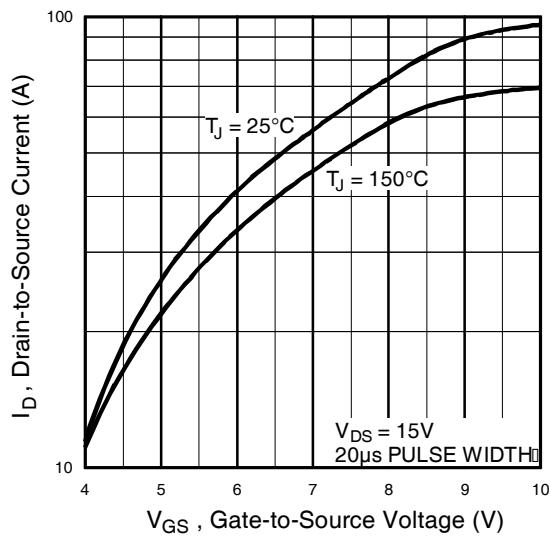
**Fig 3.** Typical Transfer Characteristics
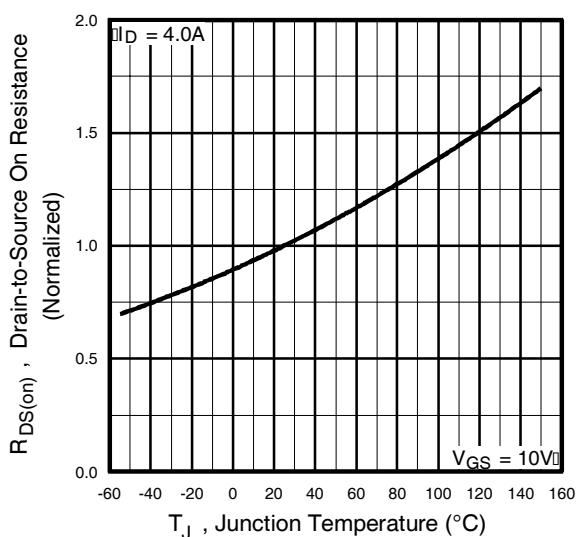
Fig 4. Normalized On-Resistance
Vs. Temperature
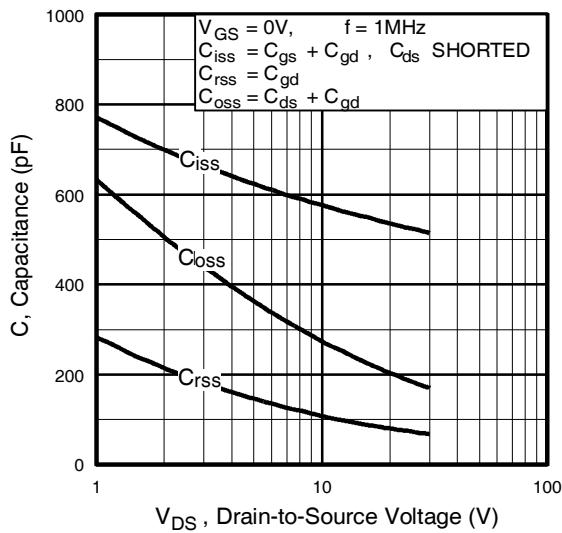
Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage
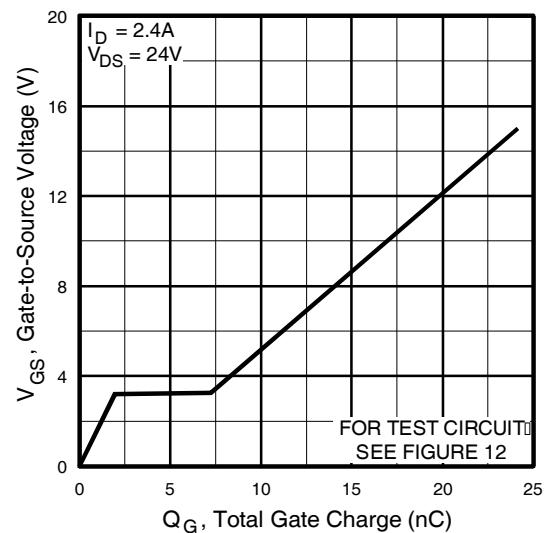

**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage
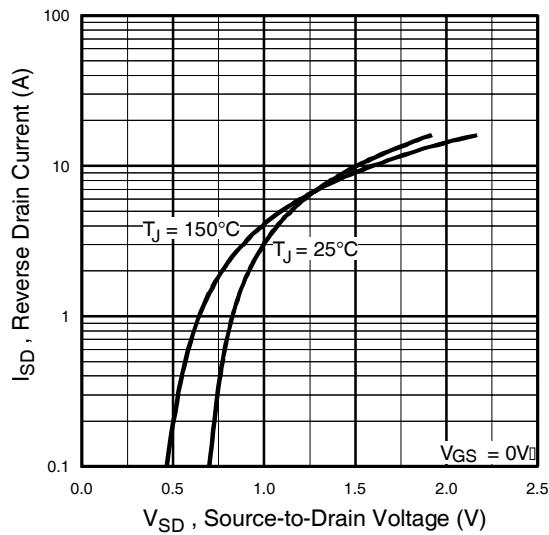
**Fig 7.** Typical Source-Drain Diode Forward Voltage
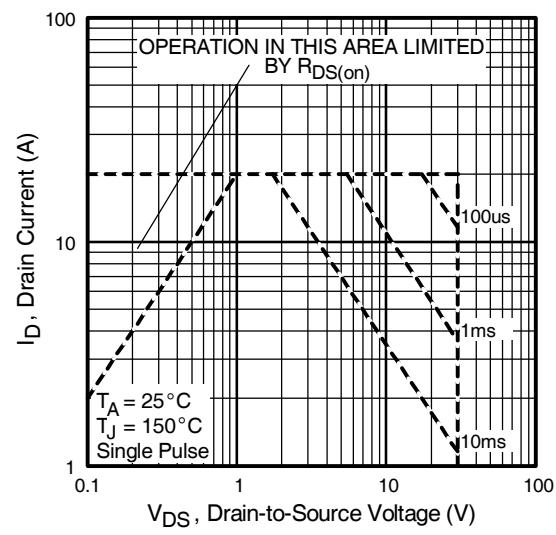

Fig 8. Maximum Safe Operating Area

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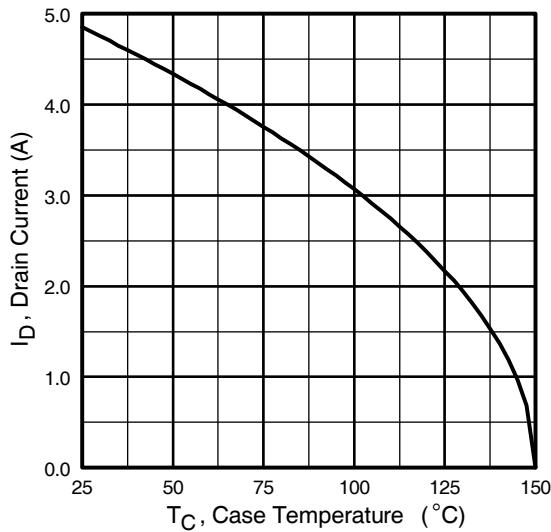
Fig 9. Maximum Drain Current Vs.
Ambient Temperature
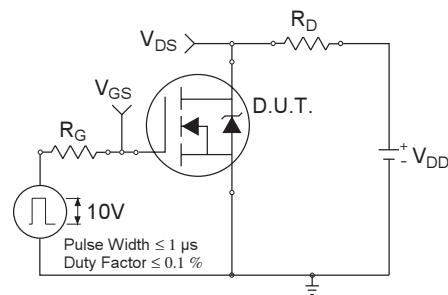
Fig 10a. Switching Time Test Circuit
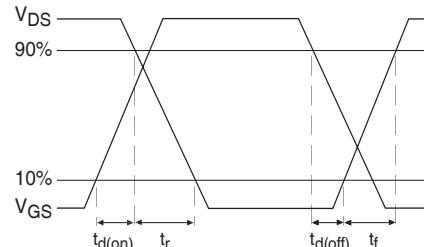
Fig 10b. Switching Time Waveforms

Notes:
1. Duty factor D = t_1 / t_2
2. Peak $T_J = P_{DM} \times Z_{thJA} + T_A$
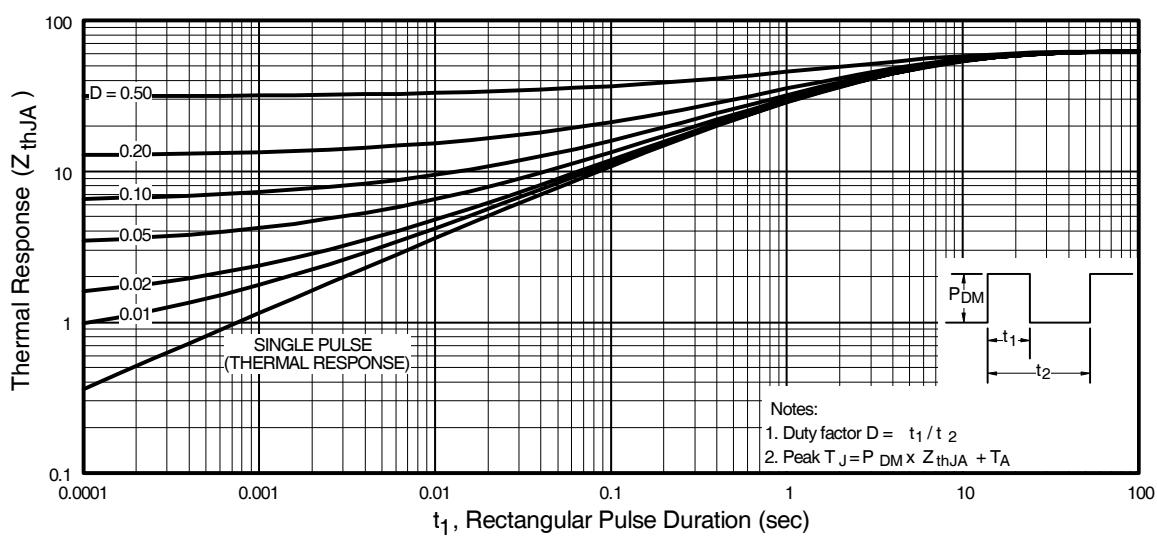
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient
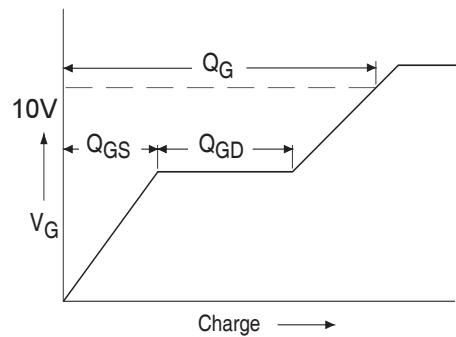
Fig 12a. Basic Gate Charge Waveform
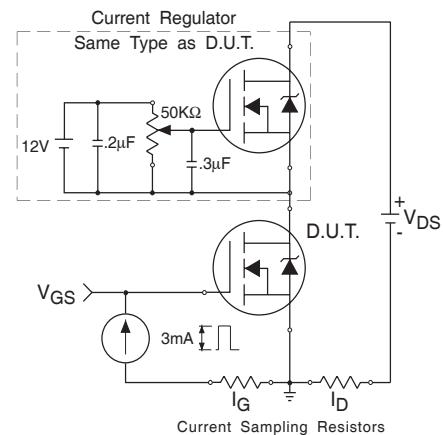
**Fig 12b.** Gate Charge Test Circuit

SOP-8
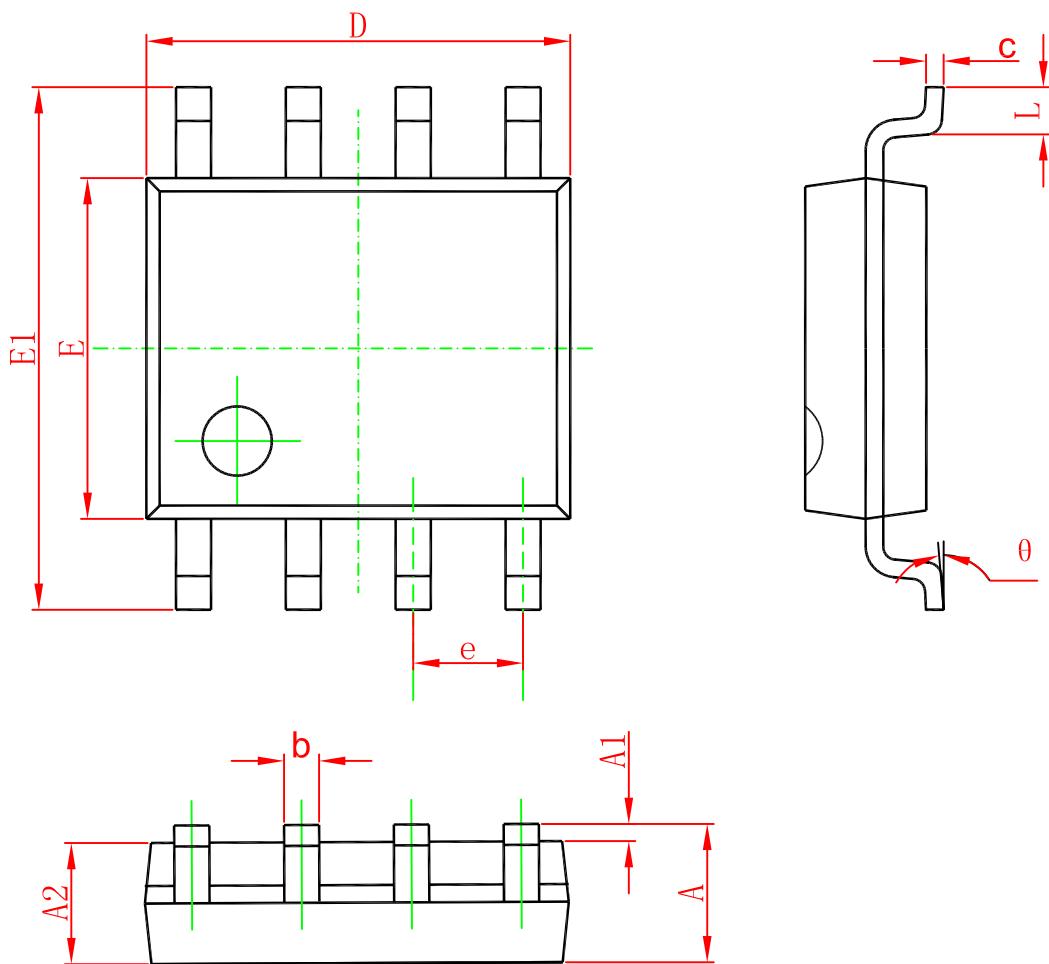
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking
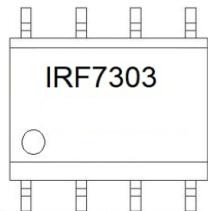
Ordering information

Order code	Package	Baseqty	Deliverymode
IRF7303TR	SOP-8	3000	Tape and reel