

Features

- 1.65-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 0.8 ns at 3.3 V
- High On-Off Output Voltage Ratio
- High Degree of Linearity
- High Speed, Typically 0.5 ns ($V_{CC} = 3$ V, $C_L = 50$ pF)
- Low ON-State Resistance, Typically $\approx 5.5 \Omega$ ($V_{CC} = 4.5$ V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

Applications

- Wireless Devices
- Audio and Video Signal Routing
- Portable Computing
- Wearable Devices
- Signal Gating, Chopping, Modulation or Demodulation (Modem)
- Signal Multiplexing for Analog-to-Digital and Digital-to-Analog Conversion Systems

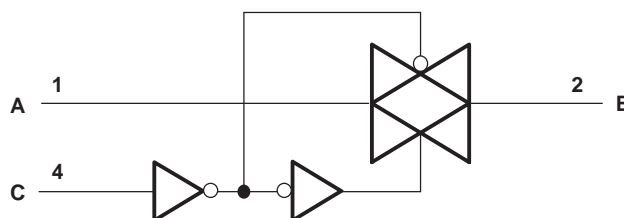
Description

This single analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

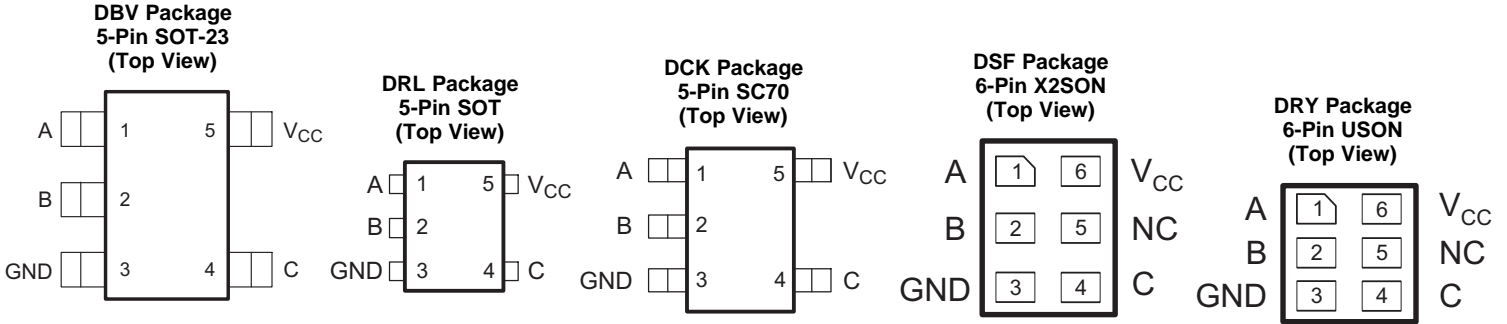
The SN74LVC1G66 device can handle analog and digital signals. The device permits bidirectional transmission of signals with amplitudes of up to 5.5 V (peak).

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

Logic Diagram (Positive Logic)



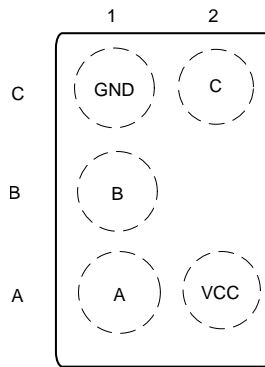
Pin Configuration and Functions



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT NO.	USON, X2SON NO.		
A	1	1	I/O	Bidirectional signal to be switched
B	2	2	I/O	Bidirectional signal to be switched
C	4	4	I	Controls the switch (L = OFF, H = ON)
GND	3	3	—	Ground pin
NC	—	5	—	Do not connect
V _{CC}	5	6	—	Power pin

**YZP Package
5-Pin DSBGA
(Bottom View)**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	DSBGA NO.		
A	A1	I/O	Bidirectional signal to be switched
B	B1	I/O	Bidirectional signal to be switched
C	C2	I	Controls the switch (L = OFF, H = ON)
GND	C1	—	Ground pin
V _{CC}	A2	—	Power pin

Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾	-0.5	6.5	V
V _I	Input voltage ⁽²⁾⁽³⁾	-0.5	6.5	V
V _{I/O}	Switch I/O voltage ⁽²⁾⁽³⁾⁽⁴⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Control input clamp current	V _I < 0	-50	mA
I _{I/O}	I/O port diode current	V _{I/O} < 0 or V _{I/O} > V _{CC}	±50	mA
I _T	ON-state switch current	V _{I/O} < 0 to V _{CC}	±50	mA
	Continuous current through V _{CC} or GND		±100	mA
T _{stg}	Storage Temperature	-65	150	°C
T _j	Junction Temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) This value is limited to 5.5 V maximum.

ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	+2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	+1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	1.65	5.5	V
V _{I/O}	I/O port voltage.	0	V _{CC}	V
V _{IH}	High-level input voltage, control input	V _{CC} = 1.65 V to 1.95 V	V _{CC} × 0.65	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	
V _{IL}	Low-level input voltage, control input	V _{CC} = 1.65 V to 1.95 V	V _{CC} × 0.35	V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.3	
V _I	Control input voltage	0	5.5	V
Δt/Δv	Control input transition rise and fall time	V _{CC} = 1.65 V to 1.95 V	20	ns/V
		V _{CC} = 2.3 V to 2.7 V	20	
		V _{CC} = 3 V to 3.6 V	10	
		V _{CC} = 4.5 V to 5.5 V	10	
T _A	Operating free-air temperature	-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Thermal Information

THERMAL METRIC	SN74LVC1G66						UNIT
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (USON)	DSF (X2SON)	YZP (DSBGA)	
	5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	5 PINS	
R _{θJA} Junction-to-ambient thermal resistance	206	252	142	—	—	132	°C/W

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP ⁽¹⁾	MAX	UNIT
r _{on} ON-state switch resistance	V _I = V _{CC} or GND, V _C = V _{IH} (see Figure 2 and Figure 1)	I _S = 4 mA	1.65 V	12	30	Ω
		I _S = 8 mA	2.3 V	9	20	
		I _S = 24 mA	3 V	7.5	15	
		I _S = 32 mA	4.5 V	5.5	10	
r _{on(p)} Peak on resistance	V _I = V _{CC} or GND, V _C = V _{IH} (see Figure 2 and Figure 1)	I _S = 4 mA	1.65 V	74.5	120	Ω
		I _S = 8 mA	2.3 V	20	30	
		I _S = 24 mA	3 V	11.5	20	
		I _S = 32 mA	4.5 V	7.5	15	
I _{S(off)} OFF-state switch leakage current	V _I = V _{CC} and V _O = GND or V _I = GND and V _O = V _{CC} , V _C = V _{IL} (see Figure 3)	T _A = 25°C	5.5 V	±1		μA
±0.1						
I _{S(on)} ON-state switch leakage current	V _I = V _{CC} or GND, V _C = V _{IH} , V _O = Open (see Figure 4)	T _A = 25°C	5.5 V	±1		μA
±0.1						
I _I Control input current	V _C = V _{CC} or GND	T _A = 25°C	5.5 V	±1		μA
±0.1						
I _{CC} Supply current	V _C = V _{CC} or GND	T _A = 25°C	5.5 V	10		μA
1						
ΔI _{CC} Supply current change	V _C = V _{CC} - 0.6 V		5.5 V	500		μA
C _{ic} Control input capacitance			5 V	2		pF
C _{io(off)} Switch input and output capacitance			5 V	6		pF
C _{io(on)} Switch input and output capacitance			5 V	13		pF

(1) T_A = 25°C

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd} ⁽¹⁾	A or B	B or A	2		1.2		0.8		0.6		ns
t _{en} ⁽²⁾	C	A or B	2.5	12	1.9	6.5	1.8	5	1.5	4.2	ns
t _{dis} ⁽³⁾	C	A or B	2.2	10	1.4	6.9	2	6.5	1.4	5	ns

(1) t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

(2) t_{PZL} and t_{PZH} are the same as t_{en}.

(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V _{CC}	TYP	UNIT
Frequency response ⁽¹⁾ (switch ON)	A or B	B or A	C _L = 50 pF, R _L = 600 Ω, f _{in} = sine wave	1.65 V	35	MHz
				2.3 V	120	
				3 V	175	
				4.5 V	195	
			C _L = 5 pF, R _L = 50 Ω, f _{in} = sine wave	1.65 V	>300	
				2.3 V	>300	
				3 V	>300	
				4.5 V	>300	
Crosstalk (control input to signal output)	C	A or B	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (square wave)	1.65 V	35	mV
				2.3 V	50	
				3 V	70	
				4.5 V	100	
Feedthrough attenuation ⁽²⁾ (switch OFF)	A or B	B or A	C _L = 50 pF, R _L = 600 Ω, f _{in} = 1 MHz (sine wave)	1.65 V	-58	dB
				2.3 V	-58	
				3 V	-58	
				4.5 V	-58	
			C _L = 5 pF, R _L = 50 Ω, f _{in} = 1 MHz (sine wave)	1.65 V	-42	
				2.3 V	-42	
				3 V	-42	
				4.5 V	-42	
Sine-wave distortion	A or B	B or A	C _L = 50 pF, R _L = 10 kΩ, f _{in} = 1 kHz (sine wave)	1.65 V	0.1%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	
			C _L = 50 pF, R _L = 10 kΩ, f _{in} = 10 kHz (sine wave)	1.65 V	0.15%	
				2.3 V	0.025%	
				3 V	0.015%	
				4.5 V	0.01%	

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads -3 dB.

(2) Adjust f_{in} voltage to obtain 0 dBm at input.

Operating Characteristics

T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
		TYP	TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz	8	9	9	11	pF

Typical Characteristics

$T_A = 25^\circ\text{C}$

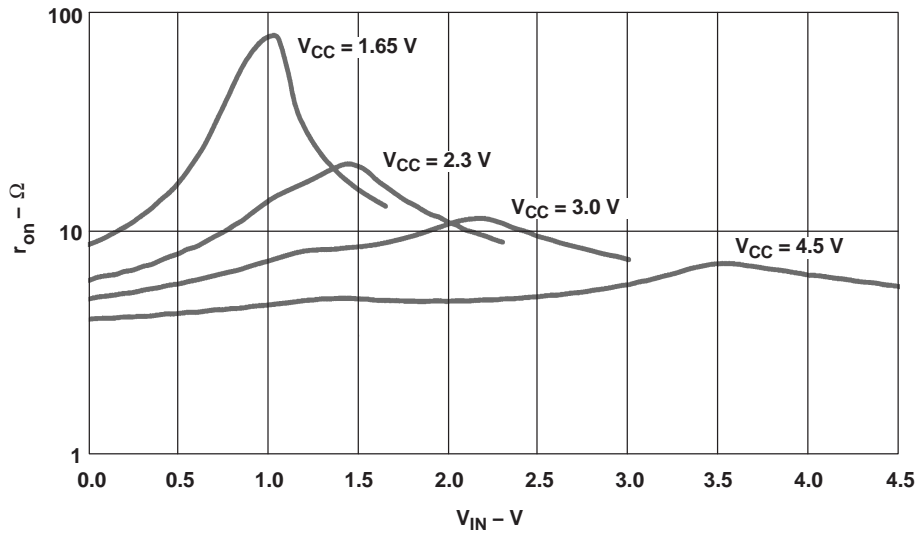


Figure 1. Typical r_{on} as a Function of Input Voltage (V_I) for $V_I = 0$ to V_{CC}

Parameter Measurement Information

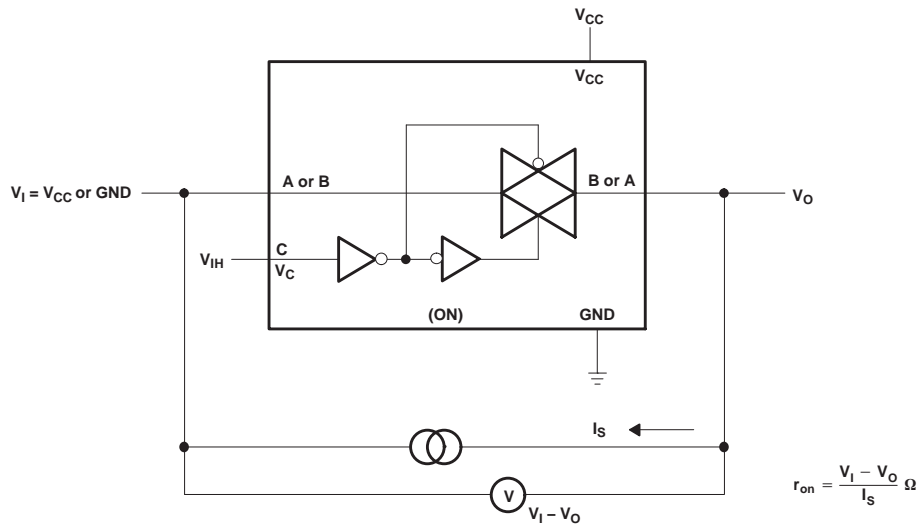


Figure 2. ON-State Resistance Test Circuit

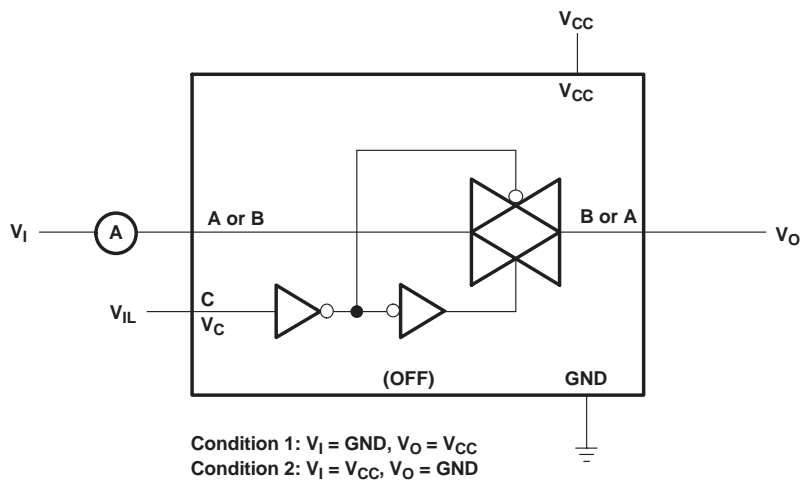


Figure 3. OFF-State Switch Leakage-Current Test Circuit

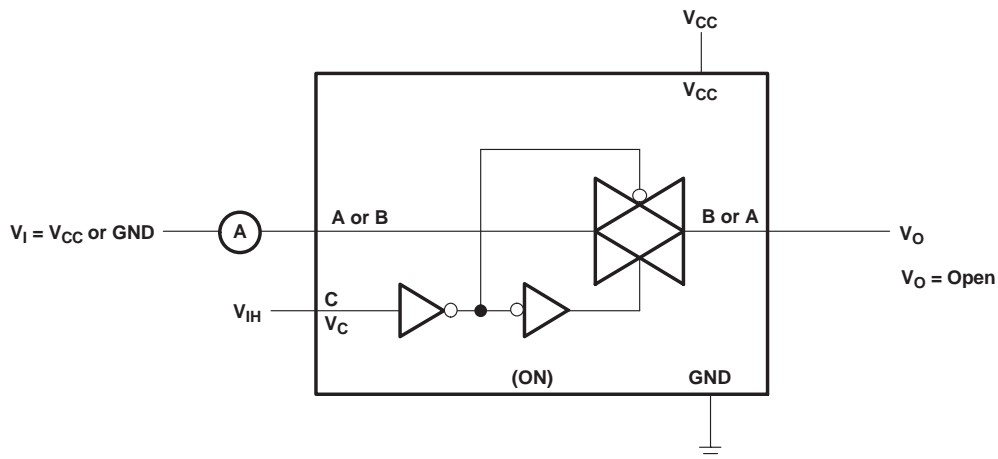
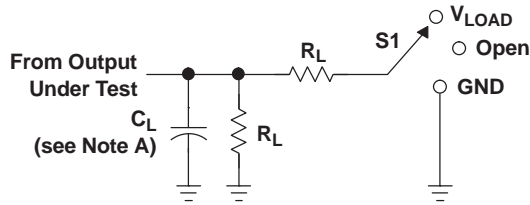


Figure 4. ON-State Switch Leakage-Current Test Circuit

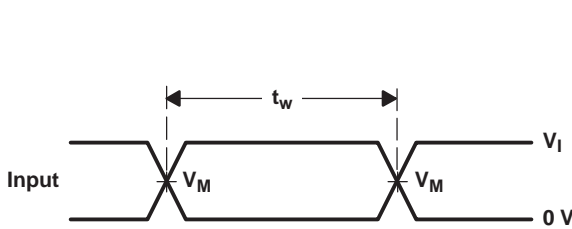
Parameter Measurement Information (continued)



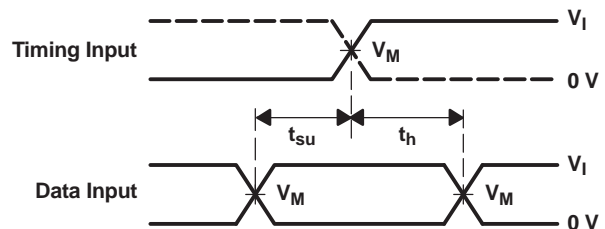
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

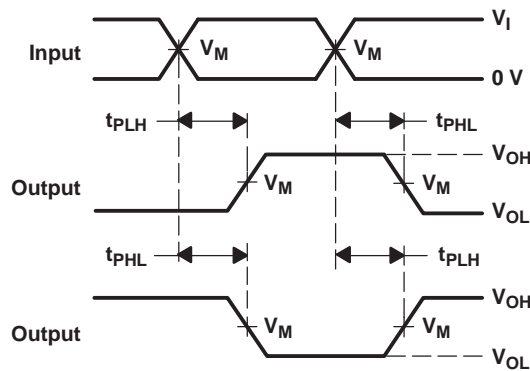
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



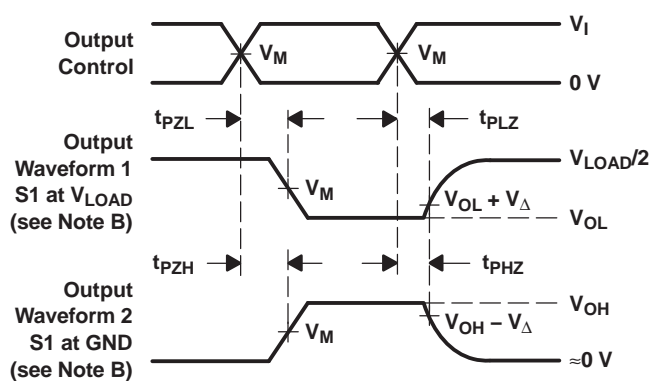
**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 5. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)

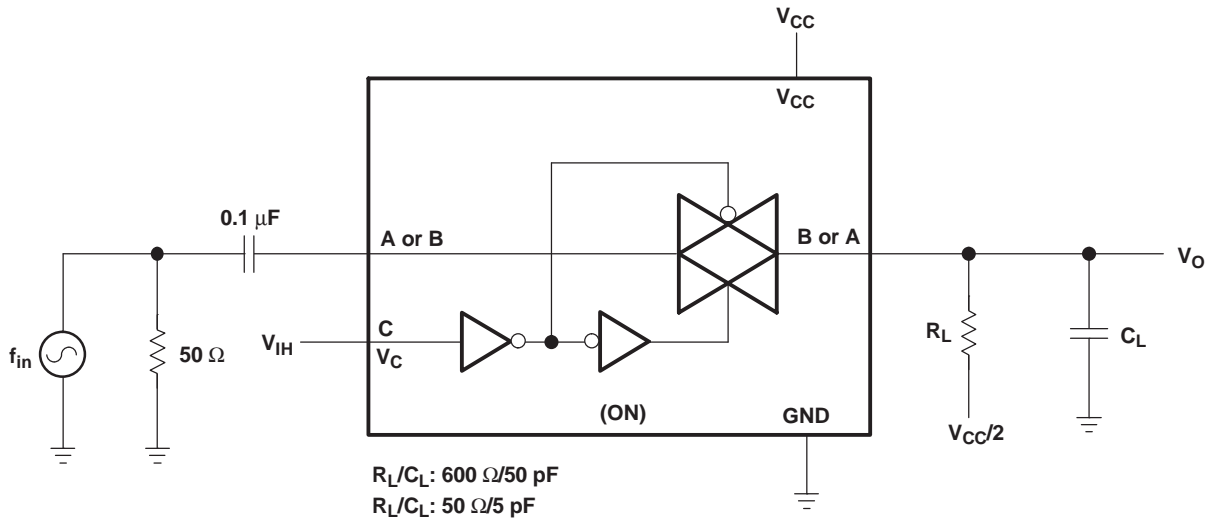


Figure 6. Frequency Response (Switch ON)

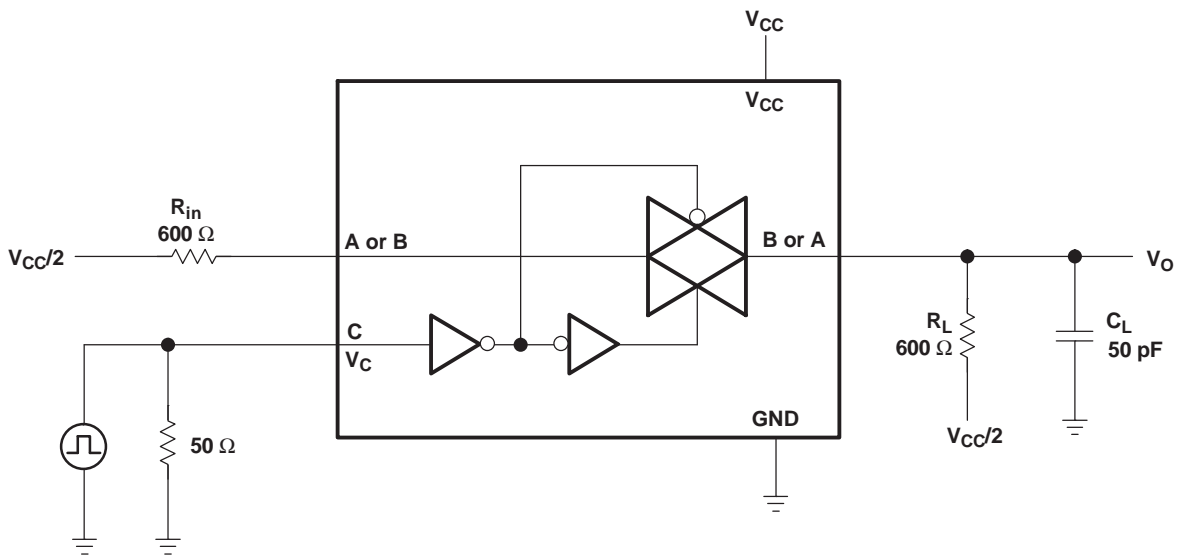


Figure 7. Crosstalk (Control Input – Switch Output)

Parameter Measurement Information (continued)

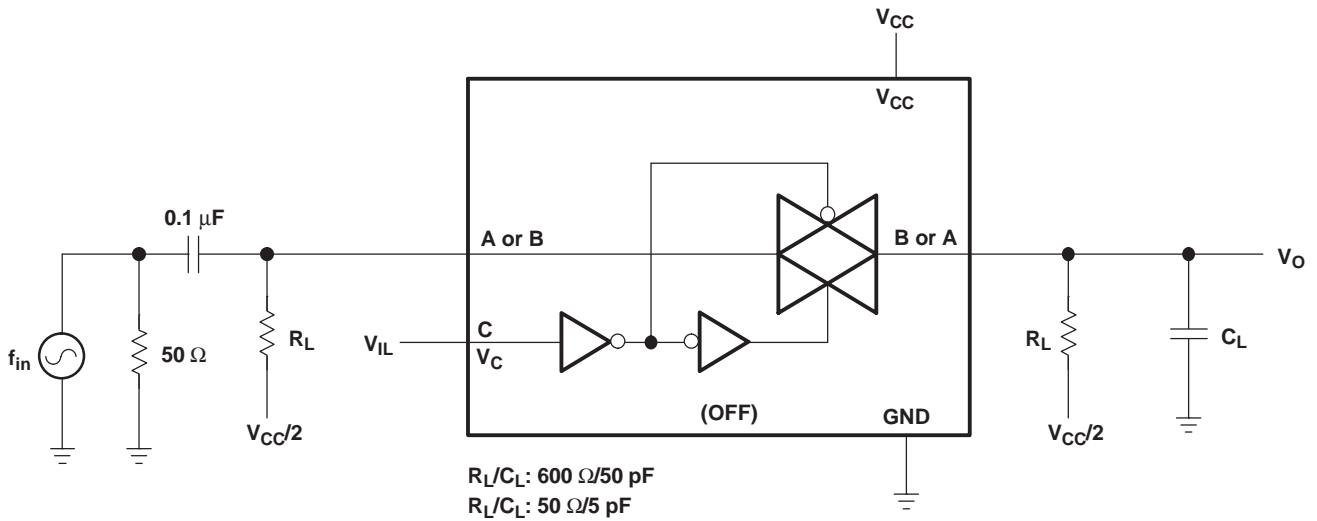


Figure 8. Feedthrough (Switch OFF)

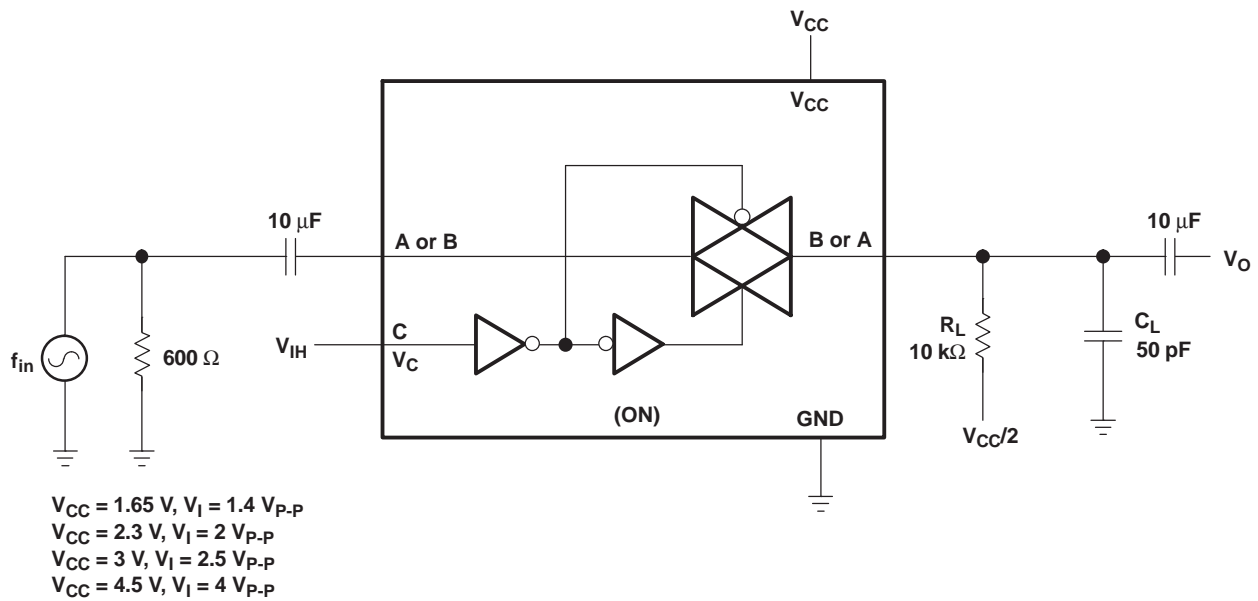


Figure 9. Sine-Wave Distortion

Detailed Description

Overview

This single analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G66 device can handle analog and digital signals. The device permits bidirectional transmission of signals with amplitudes of up to 5.5 V (peak). Like all analog switches, the SN74LVC1G66 is bidirectional.

Functional Block Diagram

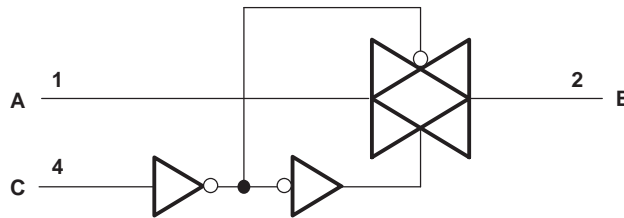


Figure 10. Logic Diagram (Positive Logic)

Feature Description

The SN74LVC1G66 has a wide V_{CC} range, allowing rail-to-rail operation of signals anywhere from a 1.8-V system to a 5-V system. In addition, the control input (C Pin) is 5.5-V tolerant, allowing higher-voltage logic to interface to the switch control system.

Device Functional Modes

Table 1. Function Table

CONTROL INPUT (C)	SWITCH
L	OFF
H	ON

Application Information

The SN74LVC1G66 can be used in any situation where an SPST switch would be used and a solid-state, voltage-controlled version is preferred.

Typical Application

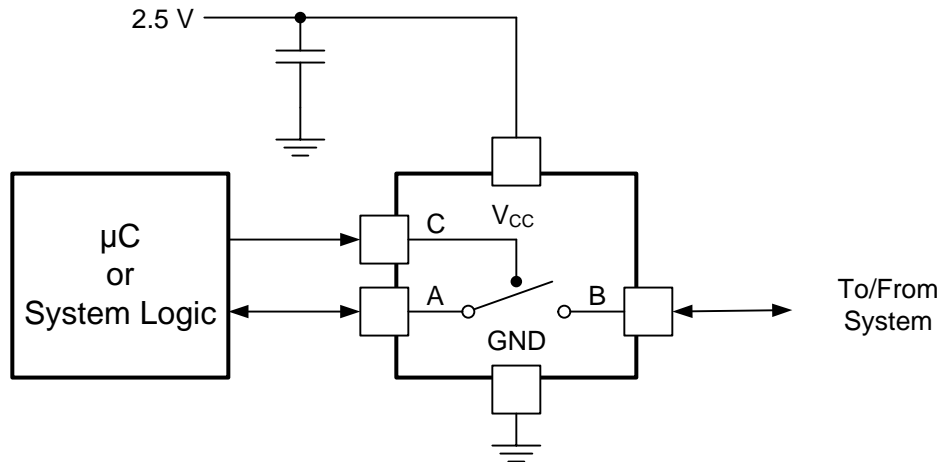


Figure 11. Typical Application Schematic

Design Requirements

The SN74LVC1G66 allows on and off control of analog and digital signals with a digital control signal. All input signals should remain between 0 V and V_{CC} for optimal operation.

Typical Application (continued)

Application Curve

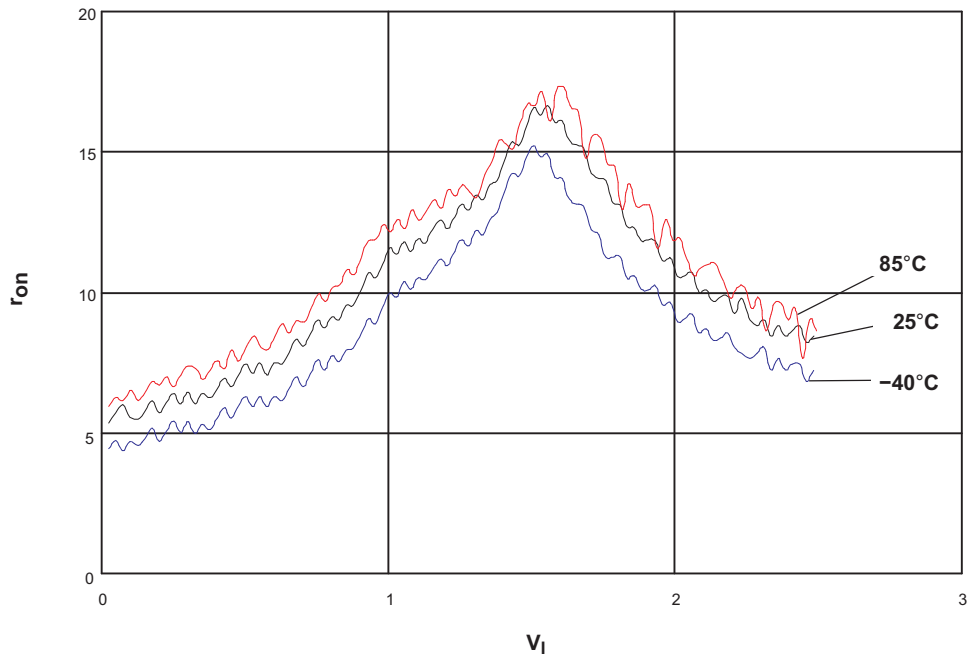
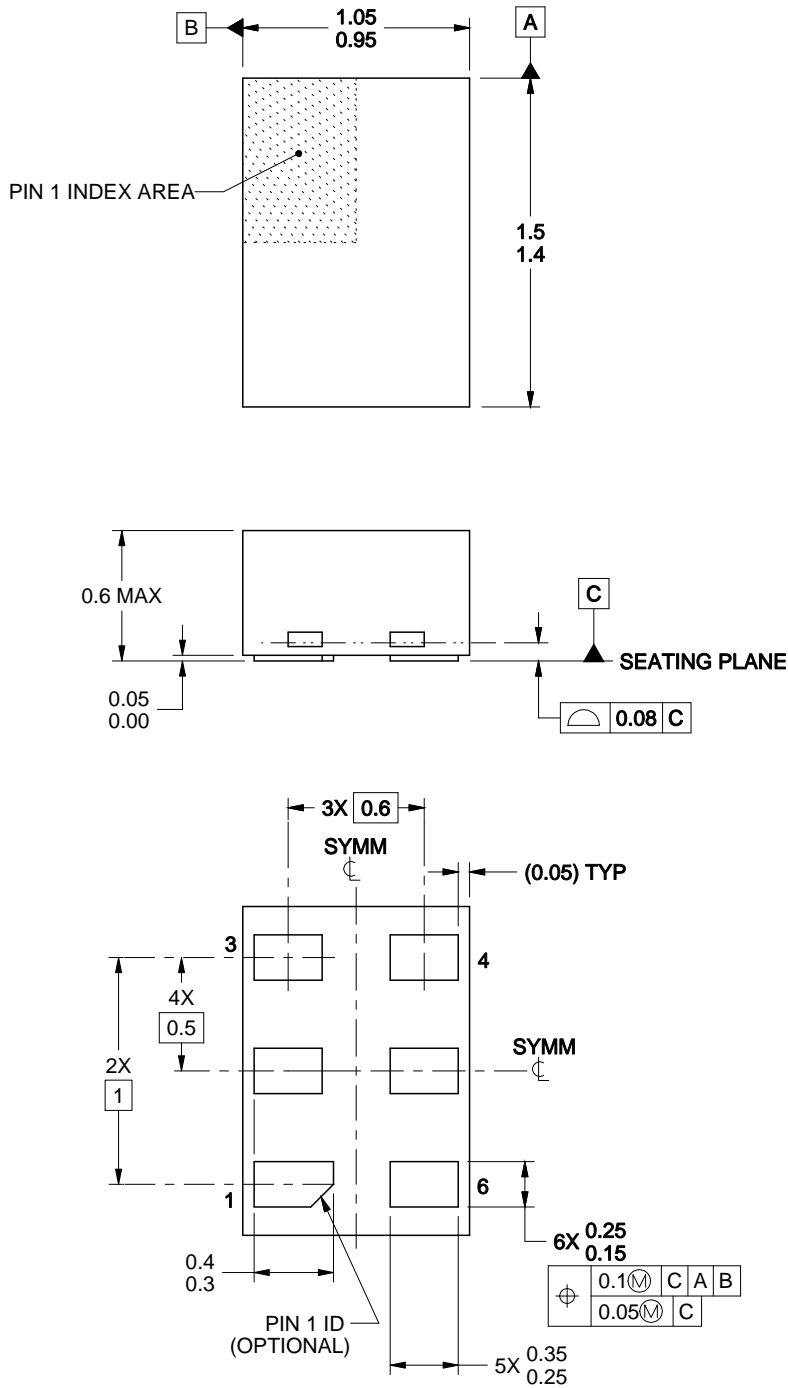


Figure 12. r_{on} vs V_I , $V_{CC} = 2.5$ V (SN74LVC1G66)

DRY (USON-6)

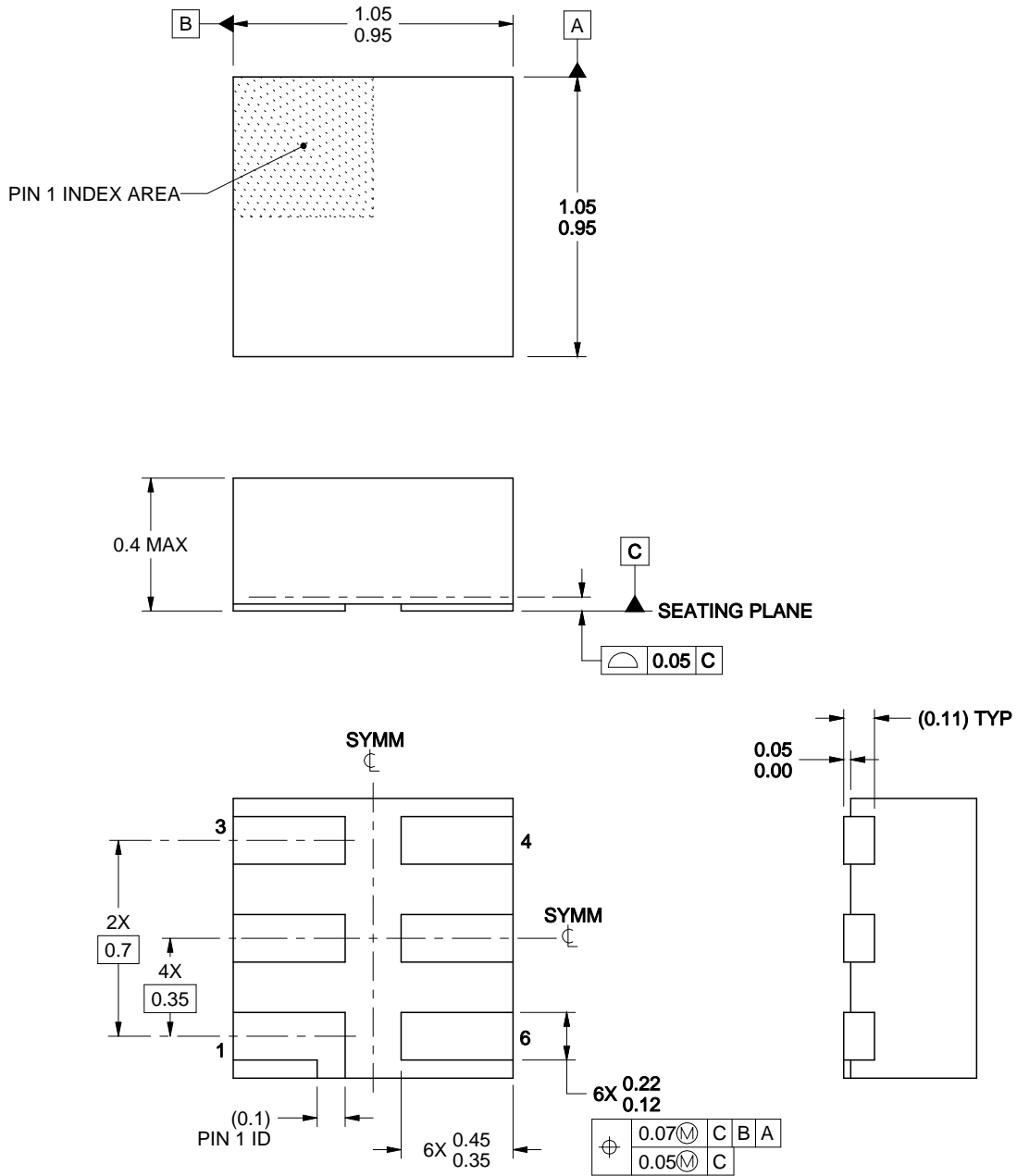


4222894/A 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

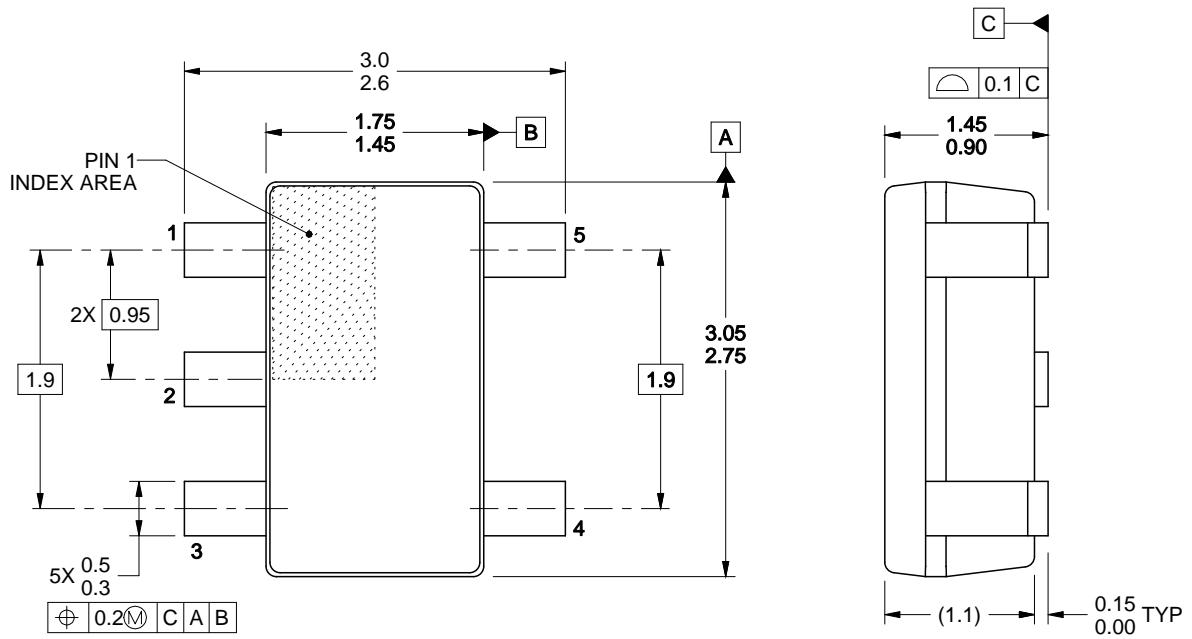
DSF (X2SON-6)



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

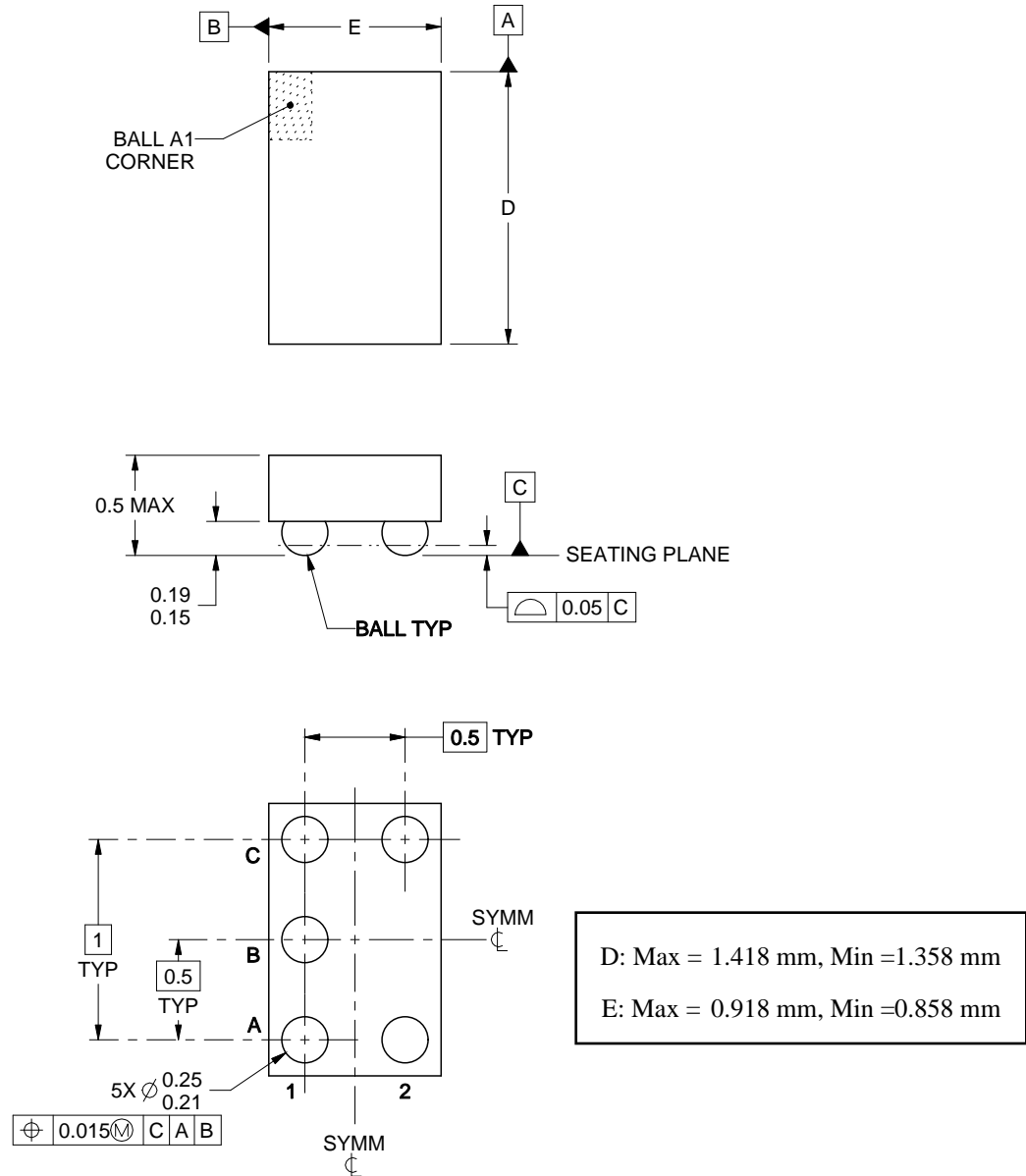
DBV (SOT23-5)



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

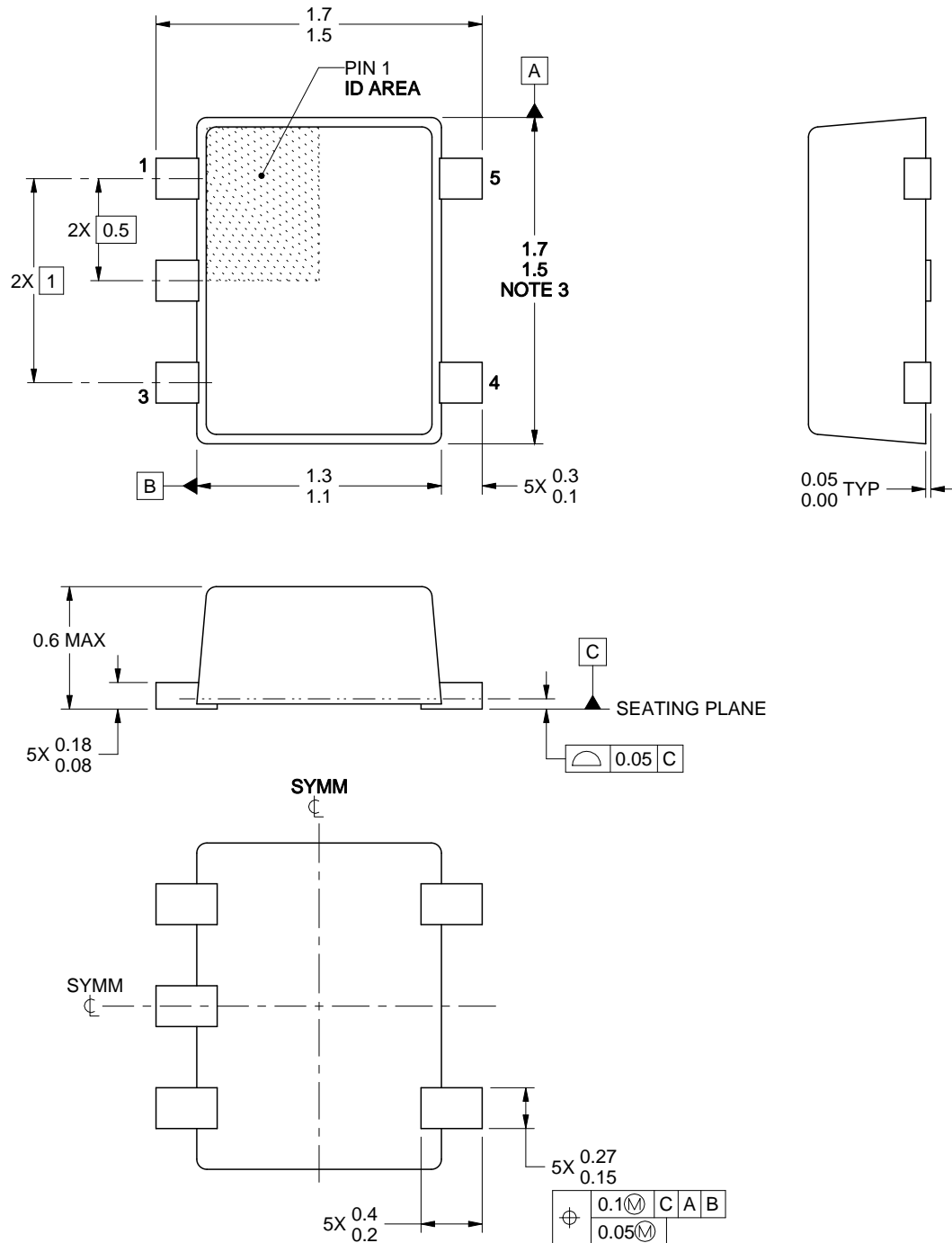
YZP (DSBGA-5)



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

DRL (SOT-553)



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

Ordering information

Order Code	Marking code	Package	Baseqty	Deliverymode
SN74LVC1G66DBVR	C665	SOT23-5	3000	Tape and reel
SN74LVC1G66DCKR	C65	SC70-5	3000	Tape and reel
SN74LVC1G66DRLR	C6R	SOT-553	3000	Tape and reel
SN74LVC1G66DRYR	C6	USON-6	3000	Tape and reel
SN74LVC1G66DSFR	C6	X2SON-6	3000	Tape and reel
SN74LVC1G66YZPR	C6N	DSBGA-5	3000	Tape and reel