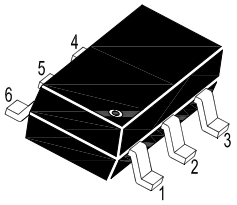
EVVOSEMI®
THINK CHANGE DO

SMF05C

TVS Diode Array
For ESD and Latch-Up Protection



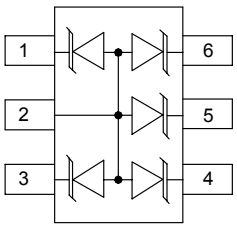
■ **Simplified outline(SOT-363)**

■ Descriptions

The SMF series TVS arrays are designed to protect sensitive electronics from damage or latch-up due to ESD and other voltage-induced transient events. They are designed for use in applications where board space is at a premium. Each device will protect up to five lines. They are unidirectional devices and may be used on lines where the signal polarities are above ground.

TVS diodes are solid-state devices designed specifically for transient suppression. They feature large cross-sectional area junctions for conducting high transient currents. They offer desirable characteristics for board level protection including fast response time, low operating and clamping voltage, and no device degradation.

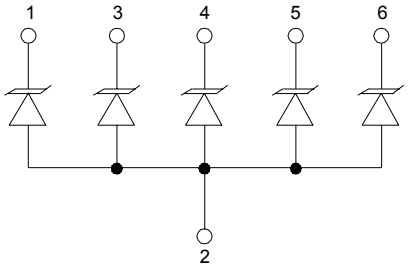
The SMF series devices may be used to meet the immunity requirements of IEC 61000-4-2, level 4. The small SC70 package makes them ideal for use in portable electronics such as cell phones, PDA's, notebook computers, and digital cameras.



Schematic & PIN Configuration

■ Features

- ◆ ESD protection for data lines to
  IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
  IEC 61000-4-4 (EFT) 40A (5/50ns)
- ◆ Small package for use in portable electronics
- ◆ Protects five I/O lines
- ◆ Working voltage: 5V
- ◆ Low leakage current
- ◆ Low operating and clamping voltages
- ◆ Solid-state silicon-avalanche technology



Circuit Diagram

■ Applications

- ◆ Cellular Handsets and Accessories
- ◆ Cordless Phones
- ◆ Personal Digital Assistants (PDA's)
- ◆ Notebooks and Handhelds
- ◆ Portable Instrumentation
- ◆ Digital Cameras
- ◆ Peripherals
- ◆ MP3 Players

■ Absolute Maximum Ratings Ta = 25℃

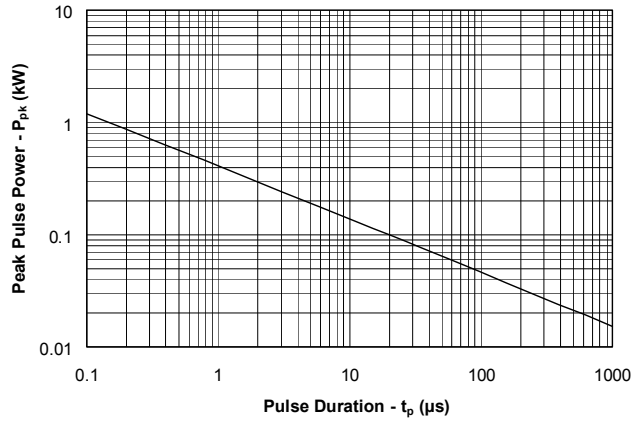
Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P_{pk}	100	Watts
Peak Pulse Current (tp = 8/20μs)	I_{PP}	8	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	20 15	kV
Lead Soldering Temperature	T_L	260 (10 seconds)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

■ Electrical Characteristics Ta = 25℃

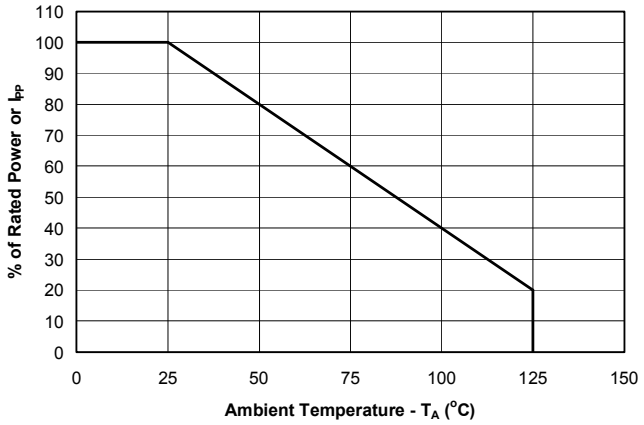
SMF05C

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	V_{RWM}				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V, T=25°C			5	μA
Clamping Voltage	V_C	I_{PP} = 5A, t_p = 8/20μs			9.8	V
Clamping Voltage	V_C	I_{PP} = 8A, t_p = 8/20μs			12.5	V
Junction Capacitance	C_j	V_R = 0V, f = 1MHz			130	pF

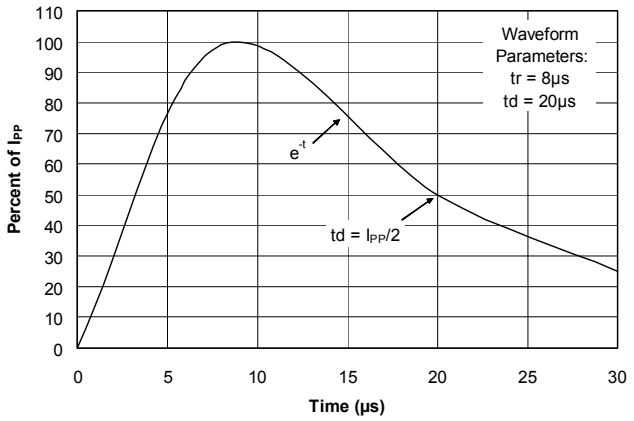
Non-Repetitive Peak Pulse Power vs. Pulse Time



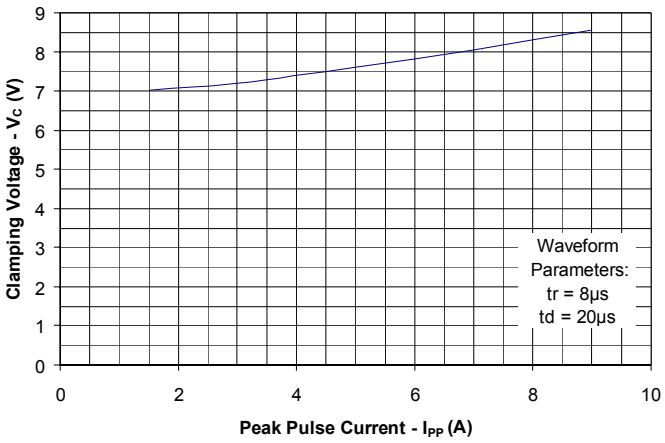
Power Derating Curve



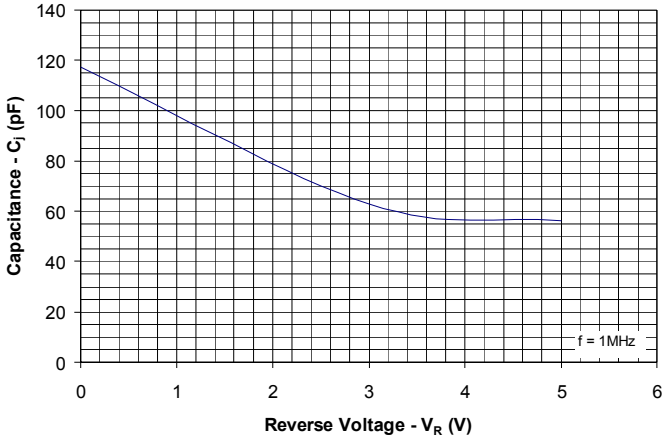
Pulse Waveform



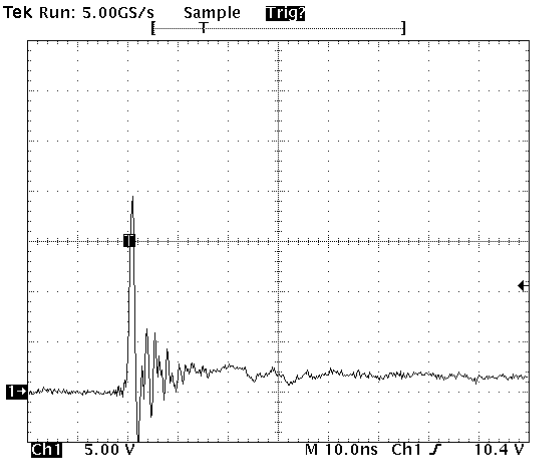
Clamping Voltage vs. Peak Pulse Current



Capacitance vs. Reverse Voltage



ESD Clamping Characteristics (8kV Contact Discharge per IEC 61000-4-2)



Device Connection for Protection of Five Data Lines

The SMF05C is designed to protect up to five unidirectional data lines. The device is connected as follows:

1. Unidirectional protection of five I/O lines is achieved by connecting pins 1, 3, 4, 5 and 6 to the data lines. Pin 2 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.

Circuit Board Layout Recommendations for Suppression of ESD.

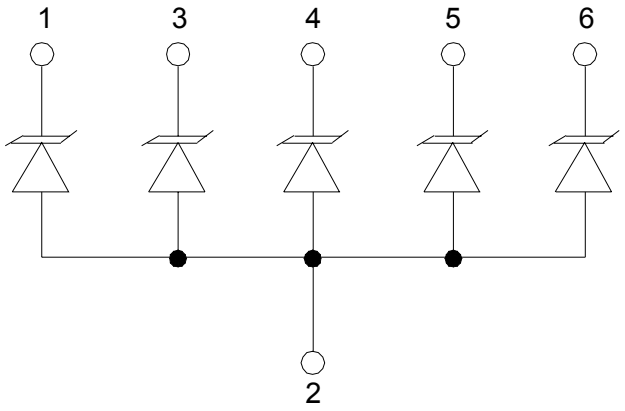
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the SMF05C near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the SMF05C and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

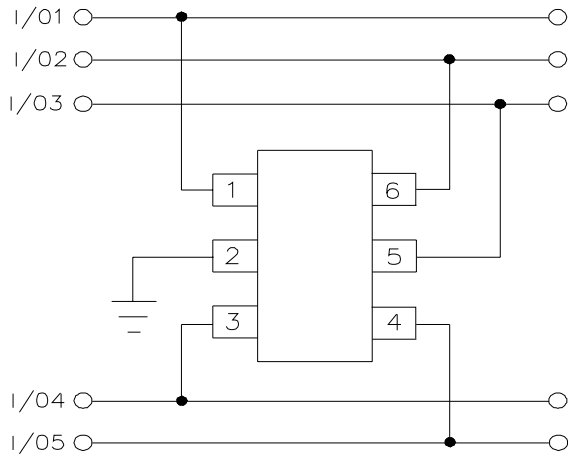
Matte Tin Lead Finish

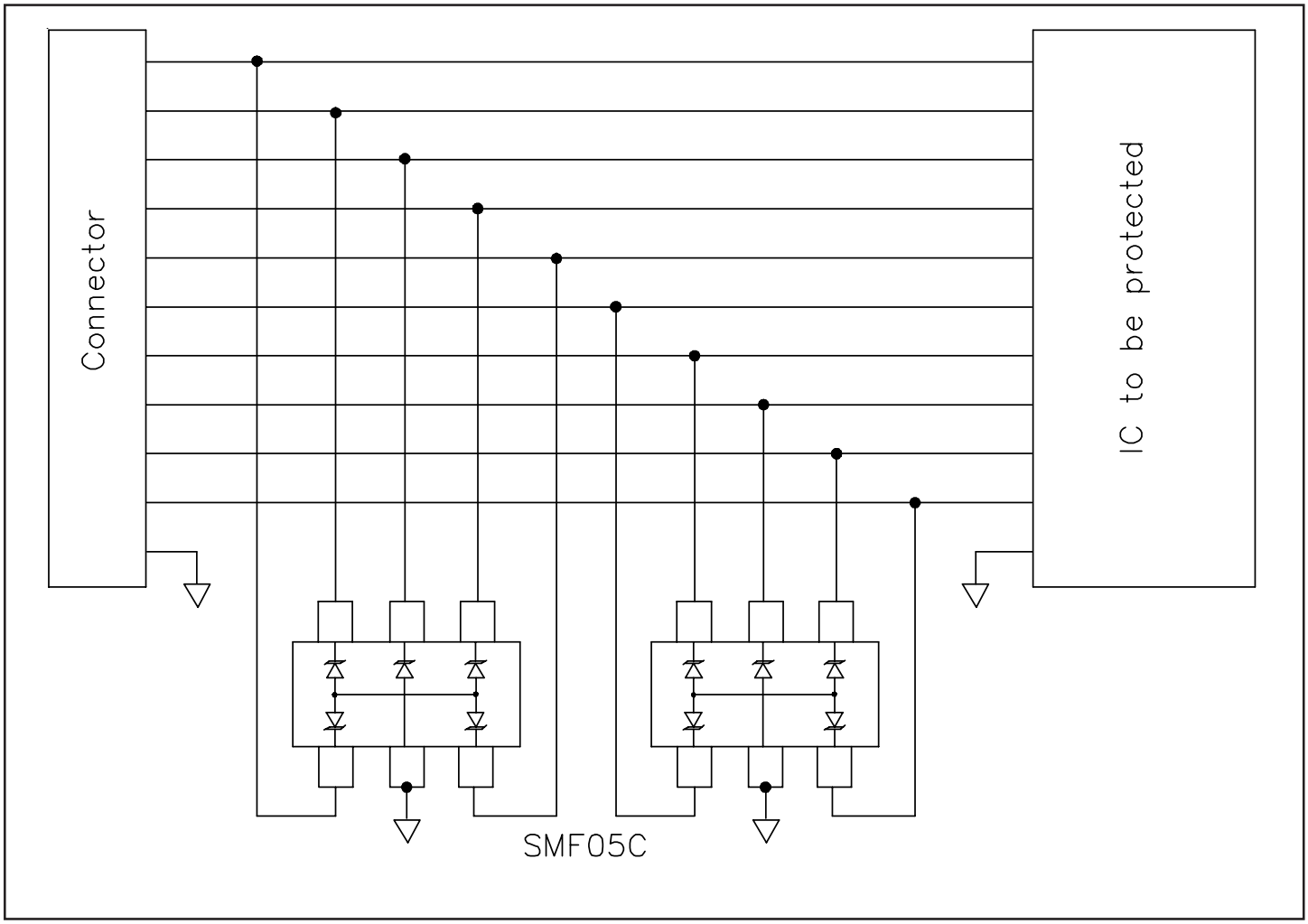
Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

SMF05C Circuit Diagram

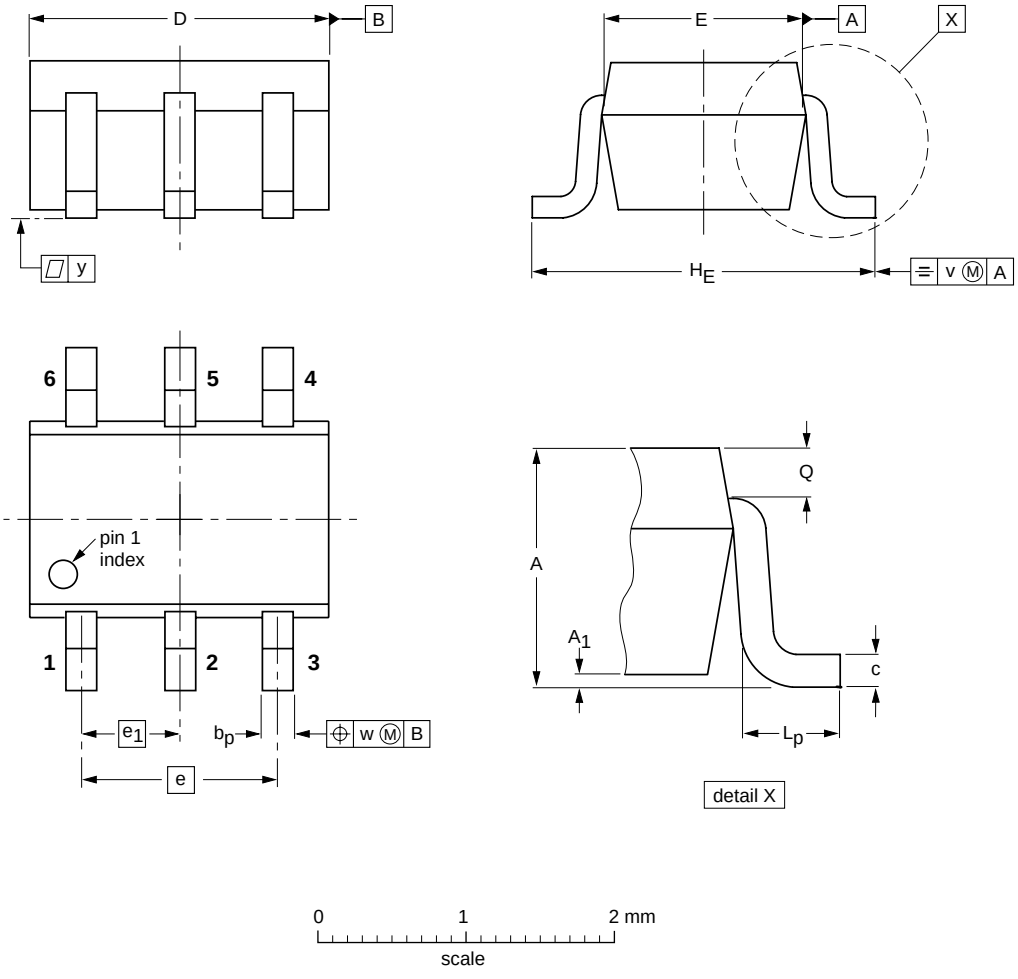


Protection of Five Unidirectional Lines




Connector
IC to be protected
SMF05C

■ SOT-363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1