

EVVOSEMI[®]

THINK CHANGE DO



ESD



TVS



MOS



LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	IRFH9310
▶ Overseas	Part Number	IRFH9310
▶ Equivalent	Part Number	IRFH9310

EV is the abbreviation of name EVVO

P-Channel Enhancement Mode MOSFET

Description

The IRFH9310 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

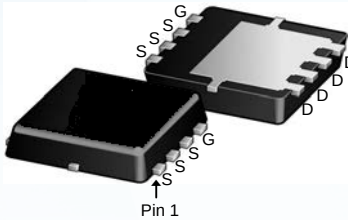
General Features

$V_{DS} = -30V$ $I_D = -90A$

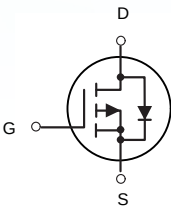
$R_{DS(ON)} < 4.5\ m\Omega$ $V_{GS} = -10V$

Application

- Battery protection
- Load switch
- Uninterruptible power supply



DFN5X6-8L



P-Channel MOSFET

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
IRFH9310	DFN5X6-8L	IRFH9310 XXXX	5000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	-90	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	-57	A
I_{DM}	Pulsed Drain Current ²	-360	A
EAS	Single Pulse Avalanche Energy ³	125	mJ
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ⁴	60	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}C$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	55	$^{\circ}C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	2.08	$^{\circ}C/W$

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Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage		$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-30	-	-	V
Gate-body Leakage current		I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
Zero Gate Voltage Drain Current	$T_J = 25^\circ\text{C}$	I_{DSS}	$V_{DS} = -30V, V_{GS} = 0V$	-	-	-1	μA
	$T_J = 100^\circ\text{C}$			-	-	-100	
Gate-Threshold Voltage		$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.0	-1.6	-2.5	V
Drain-Source On-Resistance ⁴		$R_{DS(on)}$	$V_{GS} = -10V, I_D = -30A$	-	3.5	4.5	m Ω
			$V_{GS} = -4.5V, I_D = -15A$	-	4.8	6.2	
Forward Transconductance ⁴		g_{fs}	$V_{DS} = -10V, I_D = -30A$	-	90	-	S
Input Capacitance		C_{iss}	$V_{DS} = -15V, V_{GS} = 0V, f = 1\text{MHz}$	-	5070	-	pF
Output Capacitance		C_{oss}		-	695	-	
Reverse Transfer Capacitance		C_{rss}		-	580	-	
Gate resistance		R_g	$f = 1\text{MHz}$	-	4	-	Ω
Total Gate Charge		Q_g	$V_{GS} = -10V, V_{DS} = -15V, I_D = -30A$	-	146	-	nC
Gate-Source Charge		Q_{gs}		-	21.5	-	
Gate-Drain Charge		Q_{gd}		-	39	-	
Turn-On Delay Time		$t_{d(on)}$	$V_{GS} = -10V, V_{DD} = -15V, R_G = 3\Omega, I_D = -30A$	-	23	-	ns
Rise Time		t_r		-	15	-	
Turn-Off Delay Time		$t_{d(off)}$		-	129	-	
Fall Time		t_f		-	28	-	
Diode Forward Voltage ⁴		V_{SD}	$I_S = -30A, V_{GS} = 0V$	-	-	-1.2	V
Continuous Source Current	$T_C = 25^\circ\text{C}$	I_S	-	-	-	-90	A

Note :

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$
2. The EAS data shows Max. rating . The test condition is $V_{DD} = -25V, V_{GS} = -10V, L = 0.1\text{mH}, I_{AS} = -50A$
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.

P-Channel Enhancement Mode MOSFET

Typical Characteristics

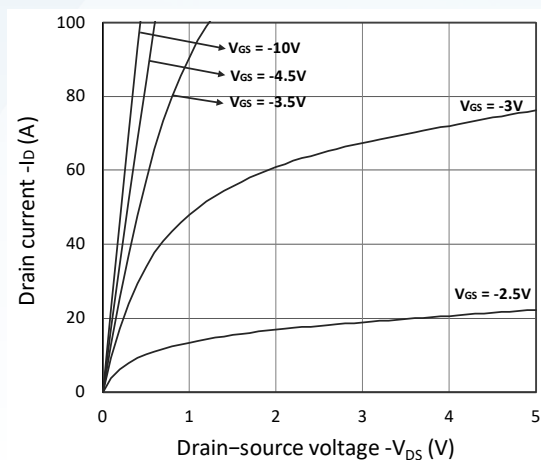


Figure 1. Output Characteristics

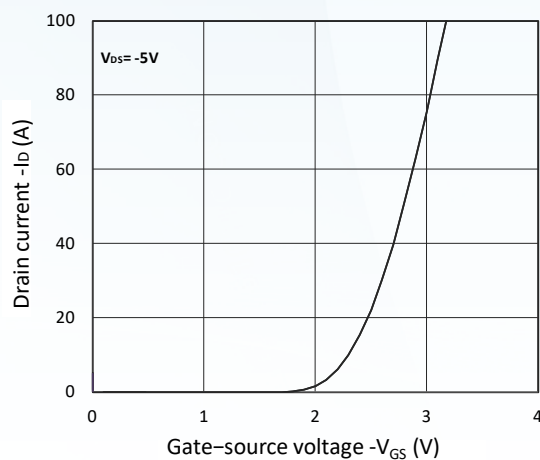


Figure 2. Transfer Characteristics

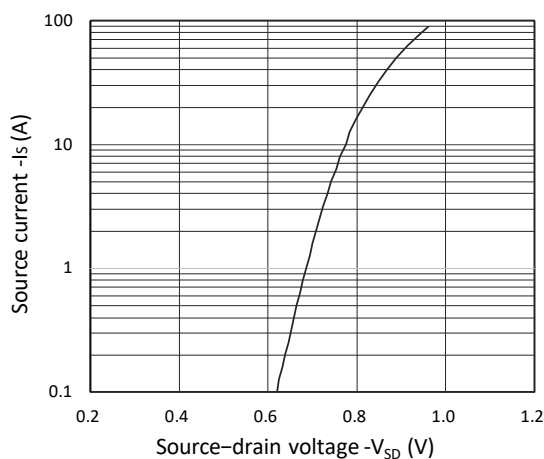


Figure 3. Forward Characteristics of Reverse

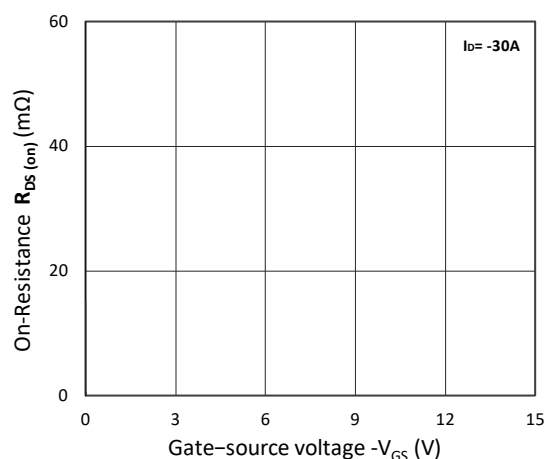


Figure 4. $R_{DS(ON)}$ vs. V_{GS}

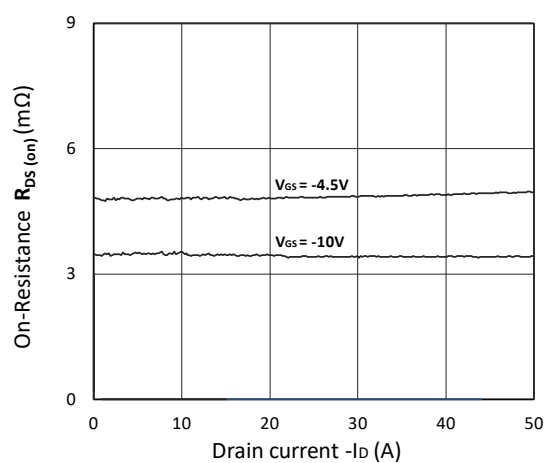


Figure 5. $R_{DS(ON)}$ vs. I_D

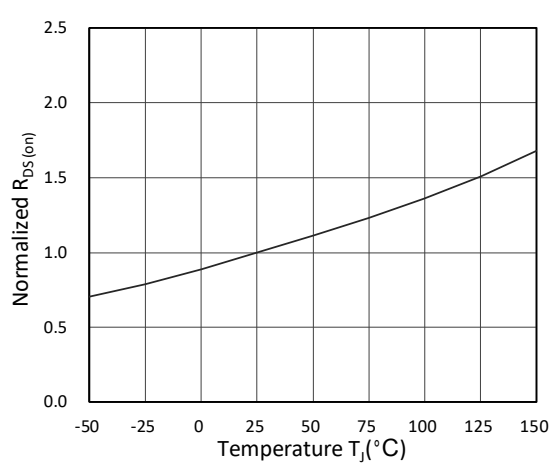


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

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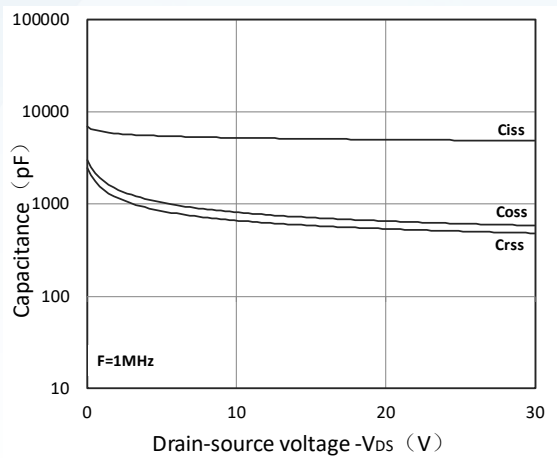


Figure 7. Capacitance Characteristics

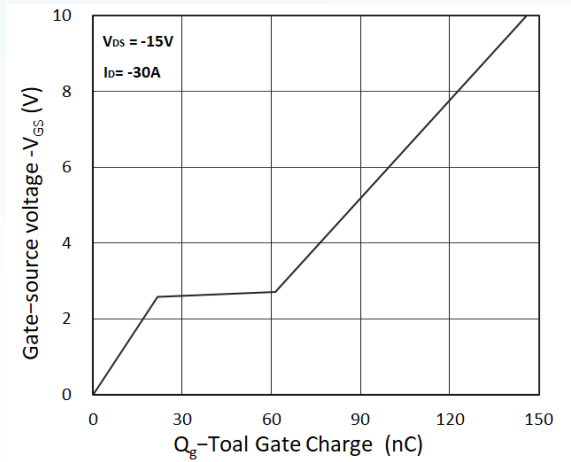


Figure 8. Gate Charge Characteristics

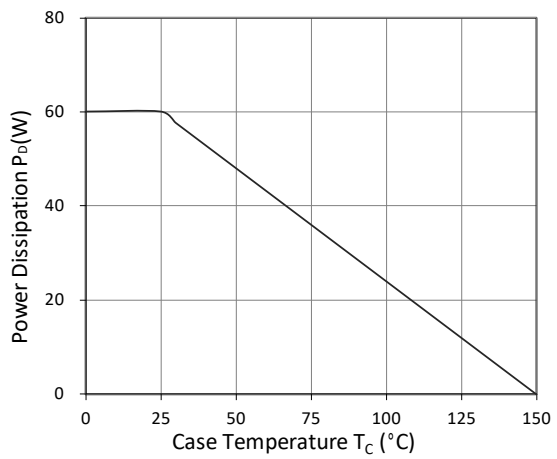


Figure 9. Power Dissipation

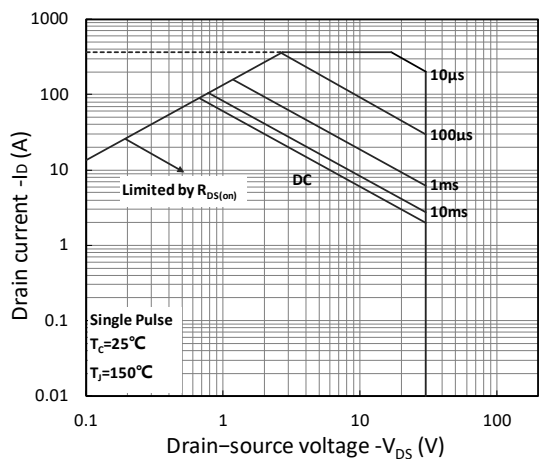


Figure 10. Safe Operating Area

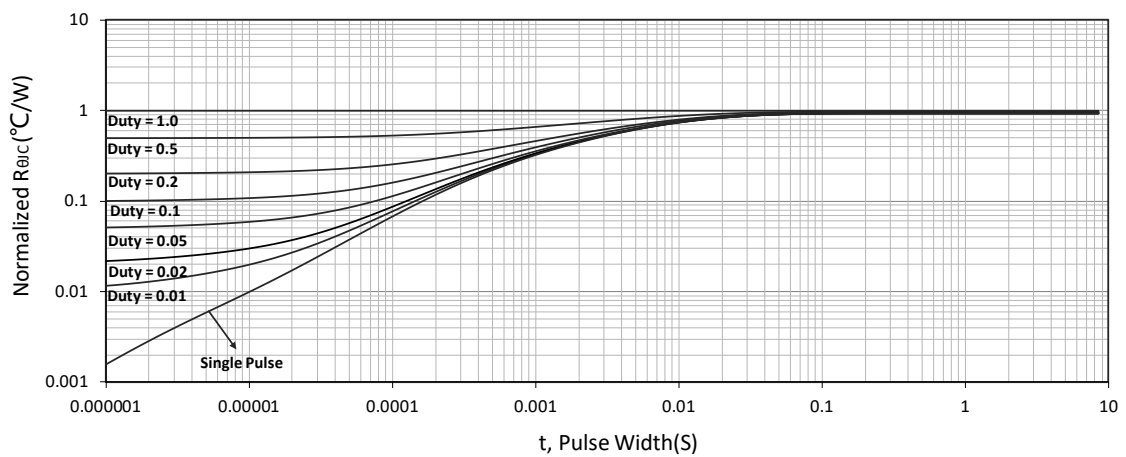


Figure 11. Normalized Maximum Transient Thermal Impedance

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Test Circuit

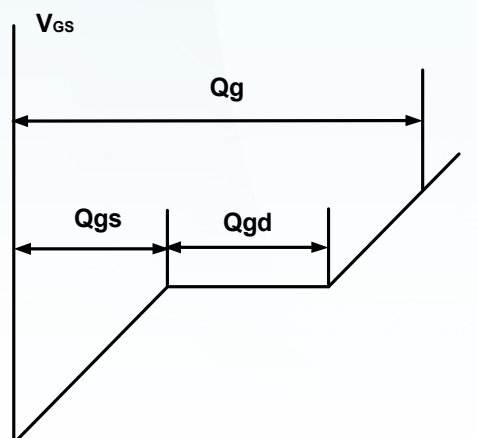
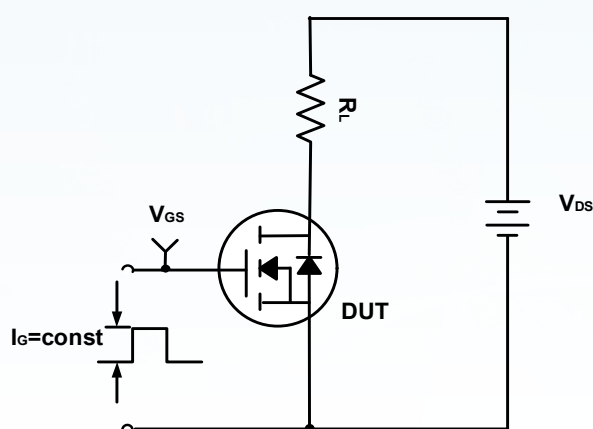


Figure A. Gate Charge Test Circuit & Waveforms

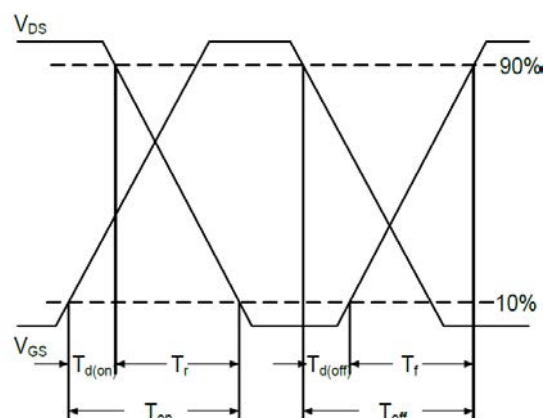
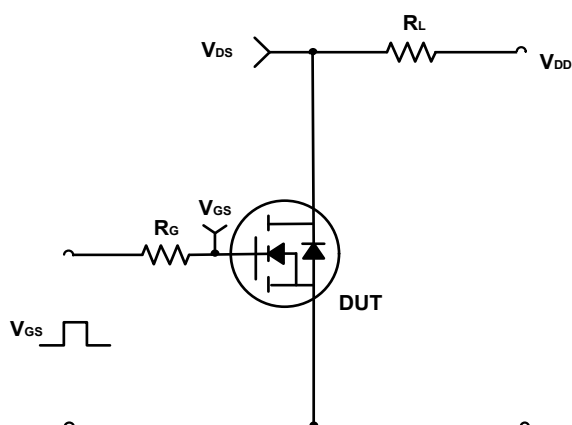


Figure B. Switching Test Circuit & Waveforms

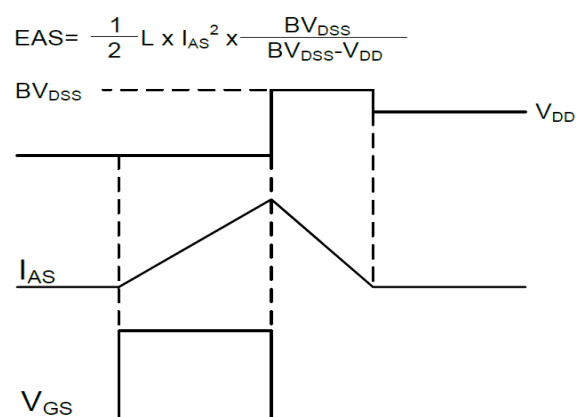
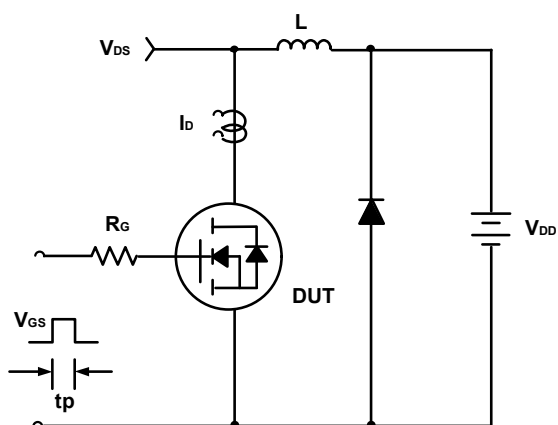
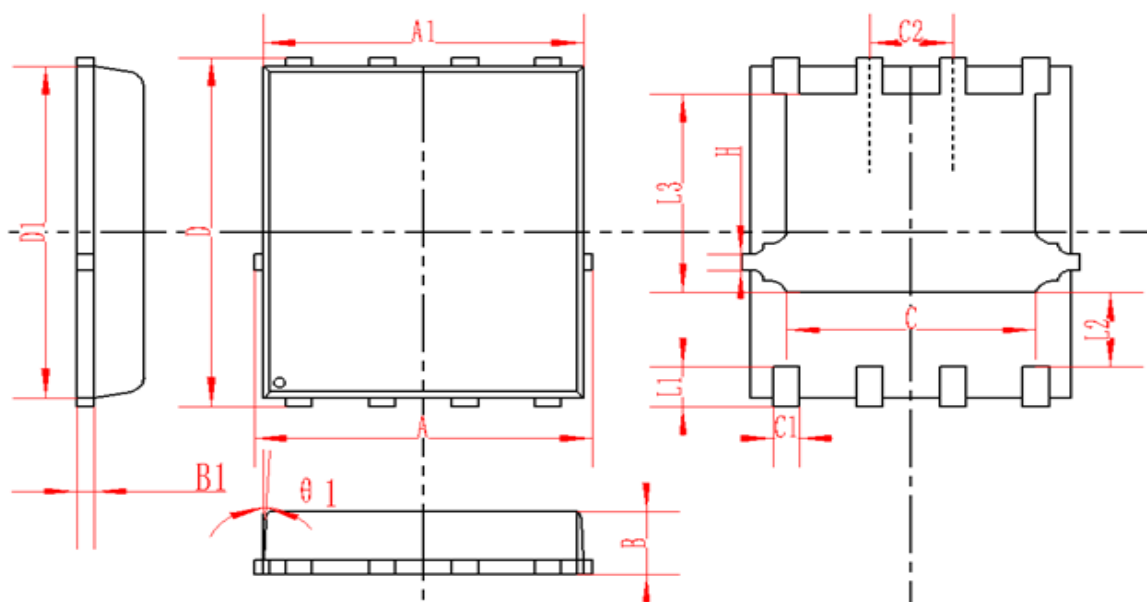


Figure C. Unclamped Inductive Switching Circuit & Waveforms

P-Channel Enhancement Mode MOSFET

DFN5X6-8L Package Information



SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.95	5	5.05	0.195	0.197	0.199
A1	4.82	4.9	4.98	0.190	0.193	0.196
D	5.98	6	6.02	0.235	0.236	0.237
D1	5.67	5.75	5.83	0.223	0.226	0.230
B	0.9	0.95	1	0.035	0.037	0.039
B1	0.254REF			0.010REF		
C	3.95	4	4.05	0.156	0.157	0.159
C1	0.35	0.4	0.45	0.014	0.016	0.018
C2	1.27TYP			0.5TYP		
θ1	8°	10°	12°	8°	10°	12°
L1	0.63	0.64	0.65	0.025	0.025	0.026
L2	1.2	1.3	1.4	0.047	0.051	0.055
L3	3.415	3.42	3.425	0.134	0.135	0.135
H	0.24	0.25	0.26	0.009	0.010	0.010

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