EVVOSEMI®
THINK CHANGE DO

ESD TVS MOS LDO Diode Sensor DC-DC

Product Specification

Domestic Part Number	IRLML5203G
Overseas Part Number	IRLML5203G
Equivalent Part Number	IRLML5203G

P-Channel Enhancement Mode Field Effect Transistor

General Description

- Trench Power LV MOSFET technology
- High density cell design for Low $R_{DS(ON)}$
- High Speed switching

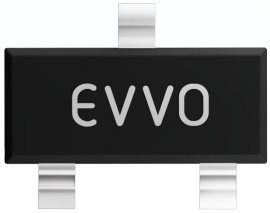
Applications

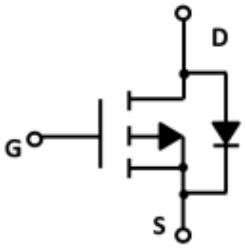
- Battery protection
- Load switch
- Power managem

Product Summary

- V_{DS} -30V
- I_D -7.9 A
- $R_{DS(ON)}$(at V_{GS}=-10V) ＜55 mohm
- $R_{DS(ON)}$(at V_{GS}=-4.5V) ＜85 mohm
- $R_{DS(ON)}$(at V_{GS}=-2.5V) ＜200 mohm

SOT-23 Pin Configuration





Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Maximum	Unit
Drain-source Voltage	V_{DS}	-30	V
Gate-source Voltage	V_{GS}	±20	V
Drain Current	I_D	-7.9	A
Pulsed Drain Current[A]	I_{DM}	-30	A
Total Power Dissipation @ T_A=25℃	P_D	1.4	W
Thermal Resistance Junction-to-Ambient @ Steady State [B]	$R_{\theta JA}$	125	℃/ W
Junction and Storage Temperature Range	T_J ,T_{STG}	-55～+150	℃

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Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250μA	-30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V,V_{GS}=0V,T_C=25℃			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±12V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1.0	-1.5	-2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}= -10V, I_D=-4.2A		35	55	mΩ
		V_{GS}= -4.5V, I_D=-2.5A		60	85	
		V_{GS}= -2.5V, I_D=-1A				
Diode Forward Voltage	V_{SD}	I_S=-3.6A,V_{GS}=0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	I_S				-2.0	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-10V,V_{GS}=0V,f=1MHZ		520		pF
Output Capacitance	C_{oss}			100		
Reverse Transfer Capacitance	C_{rss}			65		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-15V,I_D=-3A		5.9		nC
Gate Source Charge	Q_{gs}			2.8		
Gate Drain Charge	Q_{gd}			1		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=-10V, V_{DS}=-15V, I_D=-1A R_{GEN}=2.5Ω		6		ns
Turn-on Rise Time	t_r			3.5		
Turn-off Delay Time	$t_{D(off)}$			20		
Turn-off Fall Time	t_f			5.0		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. Device mounted on FR-4 PCB, 1 inch x 0.85 inch x 0.062 inch.

Typical Performance Characteristics

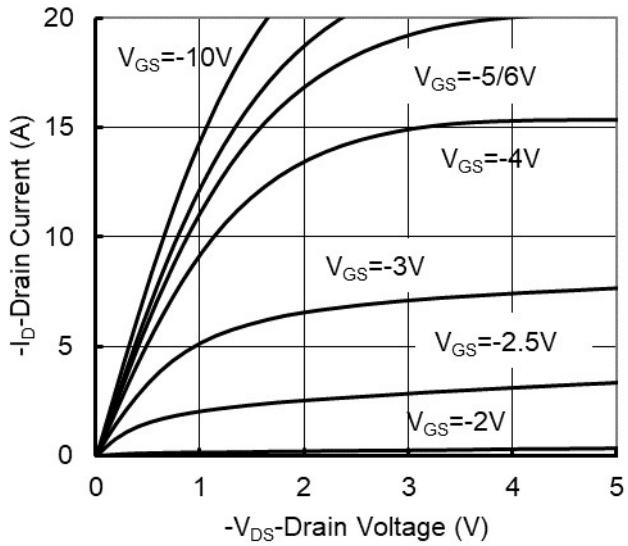

Figure1. Output Characteristics

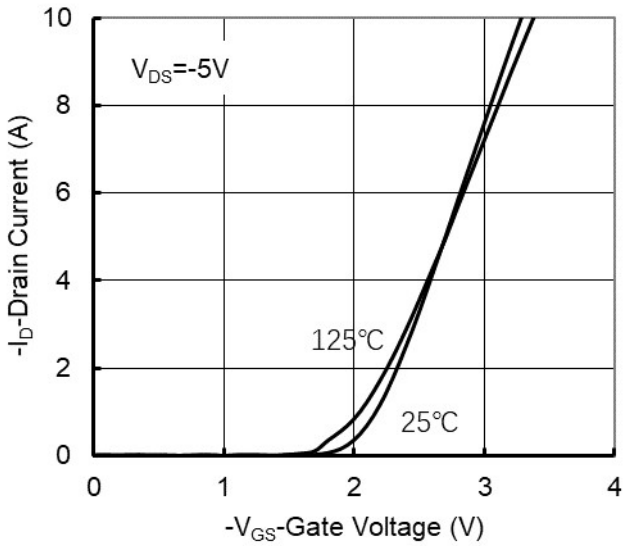

Figure2. Transfer Characteristics

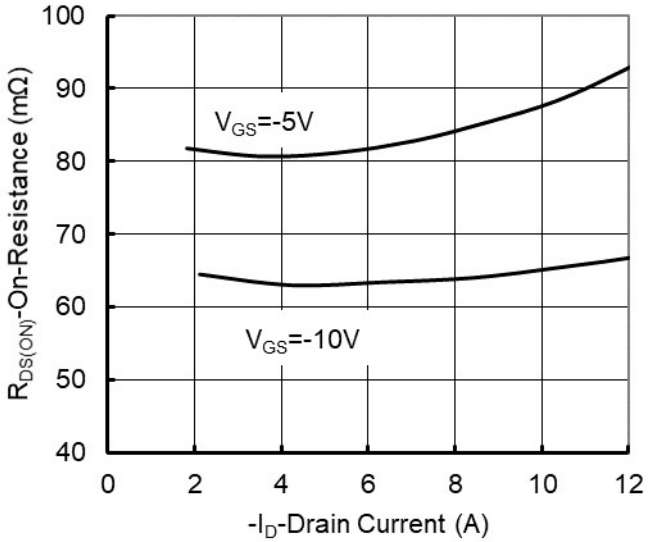

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

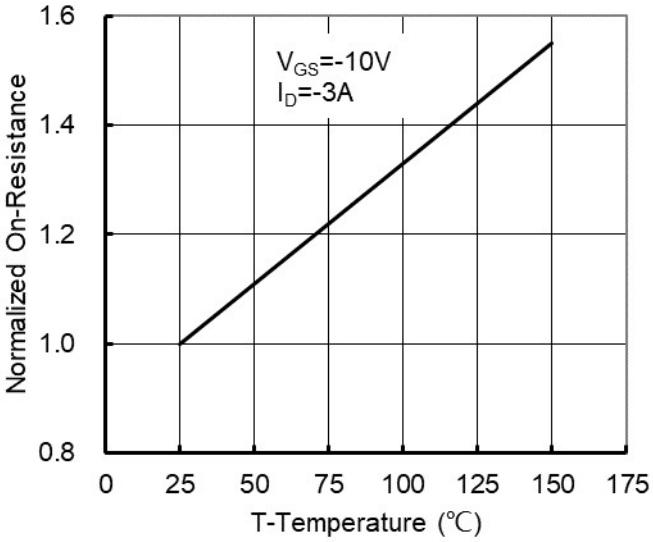

Figure 4: On-Resistance vs. Junction Temperature

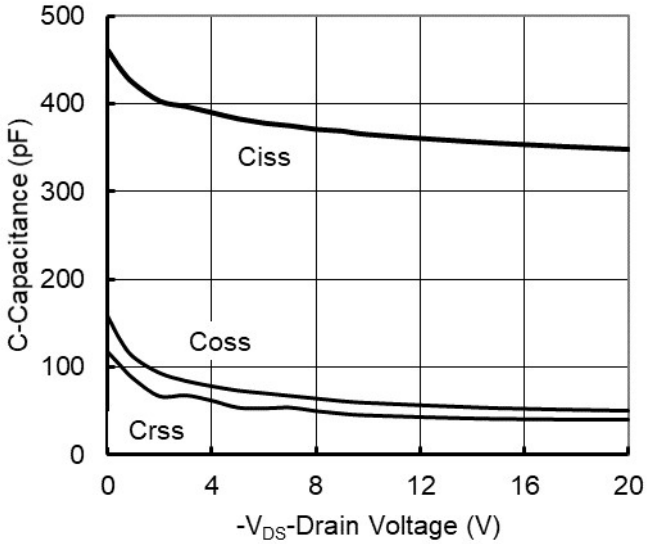

Figure5. Capacitance Characteristics

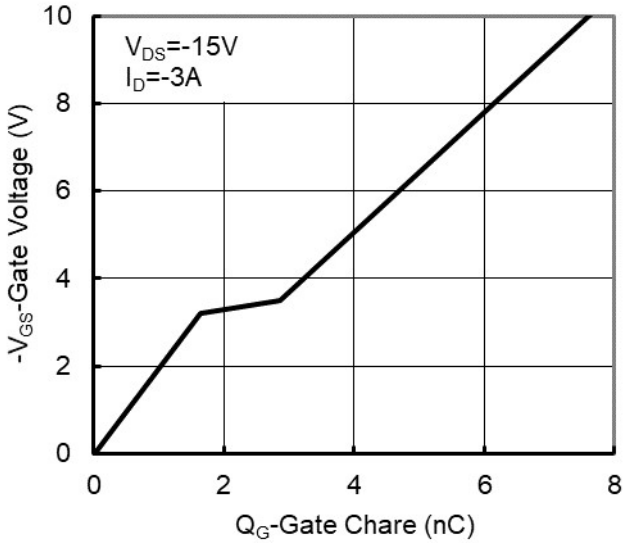

Figure6. Gate Charge

P-Channel Enhancement Mode Field Effect Transistor

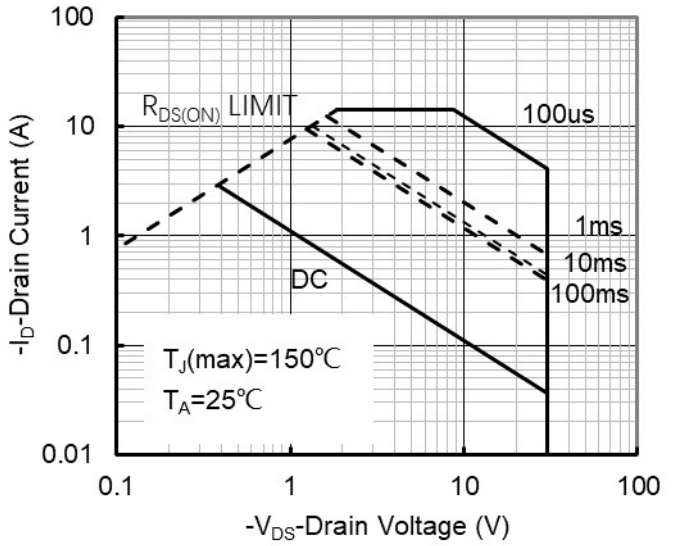

Figure7. Safe Operation Area

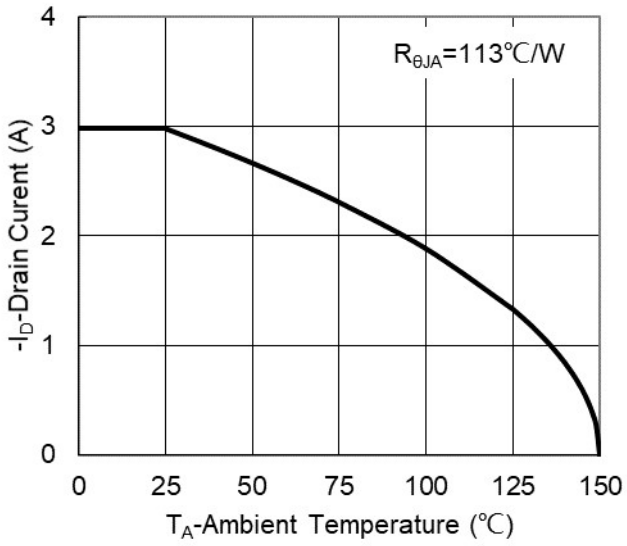

Figure8. Maximum Continuous Drain Current vs Ambient Temperature

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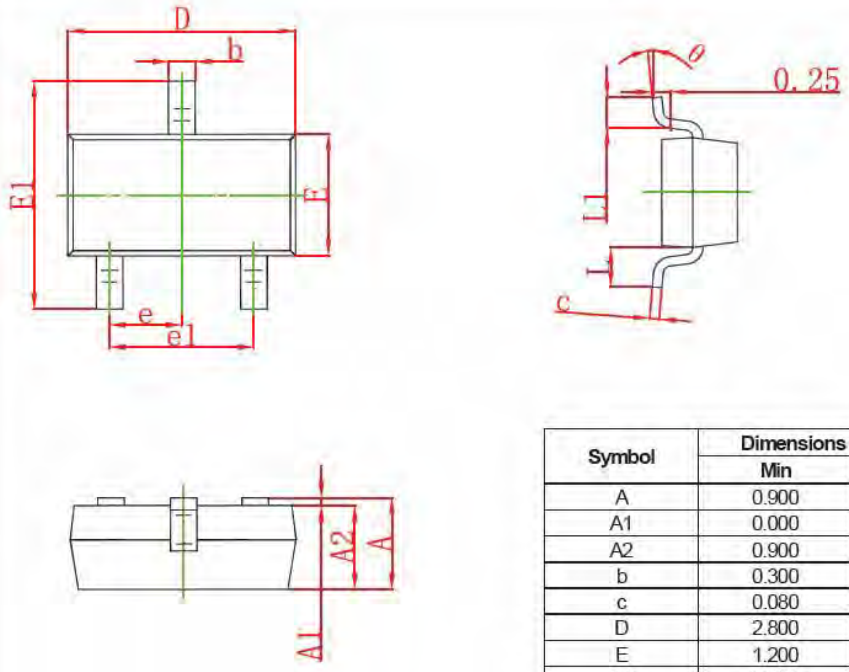
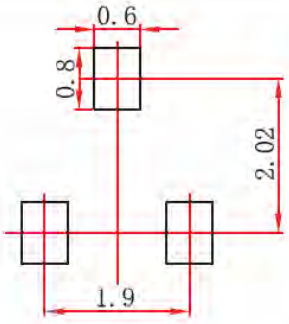
SOT-23 Package information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°

SOT-23 Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:± 0.05mm.
3.The pad layout is for reference purposes only.

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