

EVVOSEMI[®]

THINK CHANGE DO



ESD



TVS



MOS



LDO



Diode



Sensor



DC-DC

Product Specification

▶ Domestic	Part Number	HEF4052BT
▶ Overseas	Part Number	HEF4052BT
▶ Equivalent	Part Number	HEF4052BT

EV is the abbreviation of name EVVO

产品简介

HEF4052BT 是一款采用先进 CMOS 技术设计的两路差分四通道多路复用器。是一个单刀四掷配置形式的模拟开关。具有两个二进制通道控制输入 (A 和 B) 以及一个使能输入 INH。两个二进制输入信号，同时控制每路开关四个通道中的一个通道开启，其余通道关闭。

产品特点

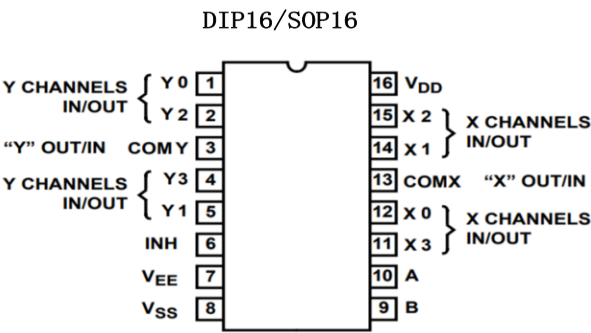
- 低输入电流： $I_{IN} \leq 1\mu A$ ， $@V_{IN}=V_{DD}-V_{SS}=15V$ ， $T_a=25^{\circ}C$
 - 低静态功耗： $I_{DD}=0.2\mu A$ (典型) $@V_{DD}-V_{SS}=15V$ ， $T_a=25^{\circ}C$
 - 低通电阻： 60Ω (典型) $@V_{DD}-V_{SS}=V_{DD}-V_{EE}=15V$ ， $T_a=25^{\circ}C$
 - 通道漏电流： $\pm 100nA$ (典型) $@V_{DD}-V_{EE}=15V$
- 宽工作电压 $V_{DD}-V_{SS}$ 范围：3V~15V
 - 先断后通切换消除了通道重迭开启
 - 单刀四掷配置形式的模拟开关
 - 封装形式：DIP16 、SOP16

产品用途

- 模拟和数字多路复用与解复用
 - 信号选通
- 数字寻址信号的逻辑电平转换
 - 其它应用领域

封装形式和管脚功能定义

管脚序号	管脚定义	说明	管脚序号	管脚定义	说明
1	Y0	Y0 通道	16	V _{DD}	电源正
2	Y2	Y2 通道	15	X2	X2 通道
3	COMY	Y 通道公共端	14	X1	X1 通道
4	Y3	Y3 通道	13	COMX	X 通道公共端
5	Y1	Y1 通道	12	X0	X0 通道
6	INH	使能控制	11	X3	X3 通道
7	V _{EE}	模拟开关负电源	10	A	地址输入 A
8	V _{SS}	电源地	9	B	地址输入 B

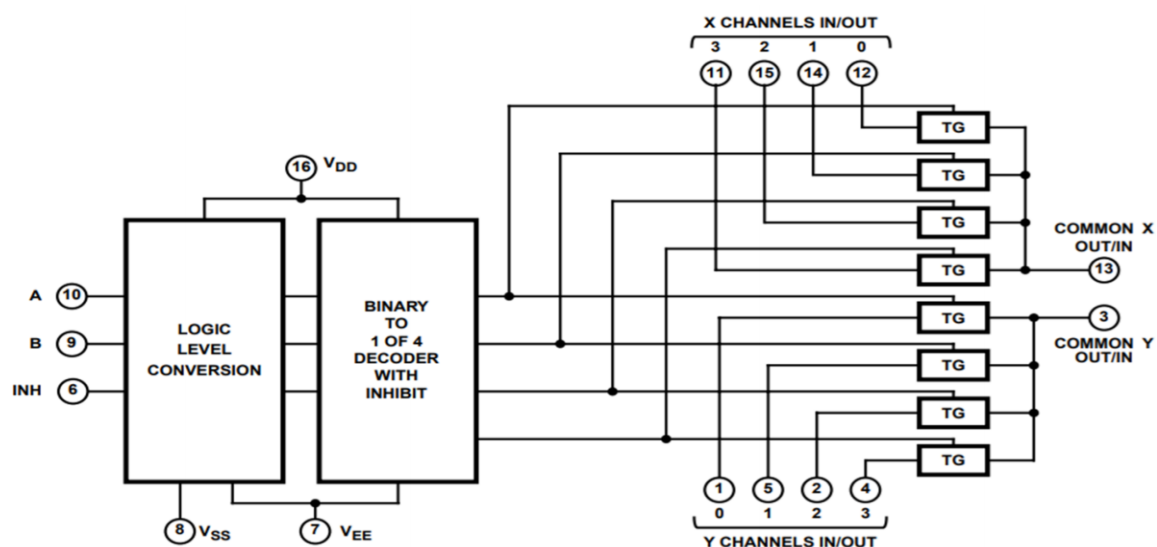


极限参数

参数	符号	极限值	单位
直流电源电压	$V_{DD}-V_{SS}$	-0.5~18	V
模拟电源电压	$V_{DD}-V_{EE}$	18	V
直流输入电压	V_{IN}	-0.5+ V_{SS} ~ V_{DD} +0.5V	V
功耗	P_D	500	mW
工作温度	T_A	0~70	°C
存储温度	T_S	-65~150	°C
引脚焊接温度	T_W	260, 10s	°C

注: 极限参数是指无论在任何条件下都不能超过的极限值。如果超过此极限值, 将有可能造成产品劣化等物理性损伤; 同时在接近极限参数下, 不能保证芯片可以正常工作。

原理逻辑图



真值表

INPUTS			OUTPUTS
INH	B	A	“ON” CHANNEL(S)
0	0	0	X0、Y0
0	0	1	X1、Y1
0	1	0	X2、Y2
0	1	1	X3、Y3
1	×	×	None

×:任意值

推荐工作条件

项目	符号	最小值	典型值	最大值	单位
直流电源电压	$V_{DD}-V_{SS}$	3		15	V
控制输入电压	V_{IS}	0		$V_{DD}-V_{SS}$	V
模拟电源电压	$V_{DD}-V_{EE}$	0		15	V
模拟输入输出电压	V_{IN}, V_{OUT}	0		$V_{DD}-V_{EE}$	V
工作温度	T_A	0		60	°C

电学特性

直流电学特性: ($V_{IS}=V_{IN}-V_{SS}$, $V_{EE}=V_{SS}$, $R_L = 3k\Omega$, $T_A=25^\circ C$ 除非特别指定)

符号	项目	测试条件		VDD (V)	最小值	典型值	最大值	单位
V _{IH}	高电平有效 输入电压	V _{IH} =V _{DD} through 1k	V _{EE} =V _{SS} , RL=1kΩ to V _{SS} , I _{IS} <2uA on all OFF Channels	5	3.5			V
				10	7			V
				15	11			V
V _{IL}	低电平有效 输入电压	V _{IL} =V _{DD} through 1k		5			1.5	V
				10			3	V
				15			4	V
R _{ON}	导通电阻	0≤V _{IS} ≤V _{DD}	5		155		Ω	
			10		85			
			15		60			
△R _{ON}	相邻通道导通电 阻差		5		15		Ω	
			10		10			
			15		5			
I _{OFF}	漏电流	输入输出通道关闭, INH=V _{DD}	18			±100	nA	
I _{IN}	输入电流	V _{IN} =V _{DD} or V _{SS}	18		0.01	±0.1	uA	
I _{DD}	静态电流	V _{IN} =V _{DD} or V _{SS}	5		0.01	5	uA	
			10		0.01	10	uA	
			15		0.01	20	uA	
C _{IN}	输入电容	任意输入端			5	7.5	pF	
C _{IS}	通道输入电容				5		pF	
C _{OS}	输出电容				9		pF	
C _{IOS}	导通电容					0.2		pF

交流电学特性: ($V_{SS}=V_{EE}$, $T_A=25^\circ C$, $tr=tf=20ns$, t_{pd} 包含 t_{PHL} , t_{PLH} , 见测试方法, 除非特别指定)

项目	符号	测试条件	VDD	最小值	典型值	最大值	单位
传输延迟时间 Signal Input to Output	t_{pd}	$V_{IS}=V_{DD}$, $R_L=200k$, $CL=50pF$	5		15		ns
			10		10		ns
			15		7		ns
传输延迟时间 Address-to-Signal OUT (Channels ON or OFF)	t_{pd}	$CL=50pF$, $R_L=10k$	5		100		ns
			10		80		ns
			15		50		ns

交流电学特性: (Continues,)

项目	符号	测试条件	VDD	最小值	典型值	最大值	单位
传输延迟时间 Inhibit-to-Signal OUT (Channel Turning ON)	tpd	C _L =50pF, R _L =1k	5		100		ns
			10		50		ns
			15		30		ns
传输延迟时间 Inhibit-to-Signal OUT (Channel Turning OFF)	tpd	C _L =50pF, R _L =10k	5		100		ns
			10		50		ns
			15		30		ns

测试方法

1、测试图

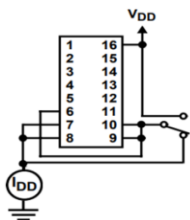


Fig. 1 静态电流

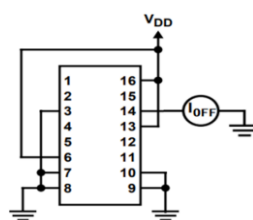


Fig. 2 相邻通道关闭漏电流

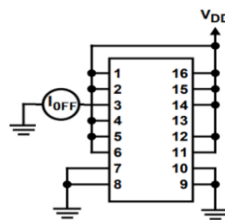


Fig. 3 所有通道关闭漏电流

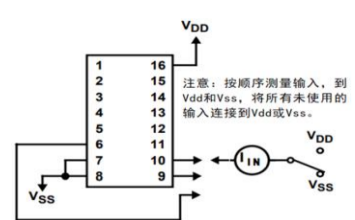


Fig. 4 输入电流

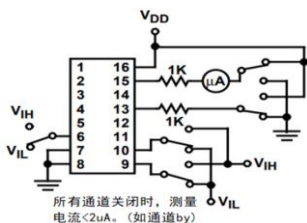


Fig. 5 输入逻辑电平电压

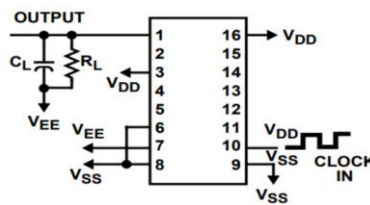


Fig. 6 传播延迟-通道控制输入 to 开关输出

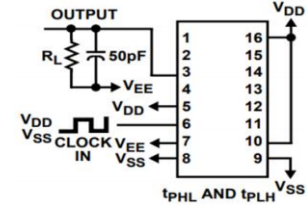


Fig. 7 传播延迟-使能输入 to 开关输出

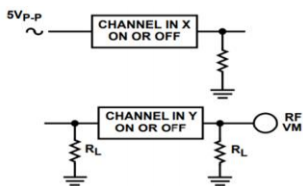


Fig. 8 相邻通道之间信号串扰

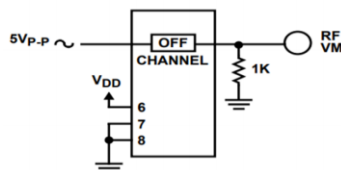


Fig. 9 所有通道关闭信号串扰

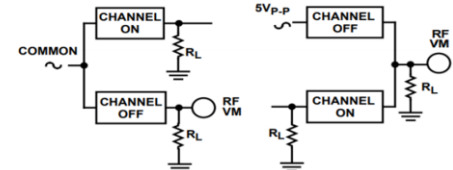
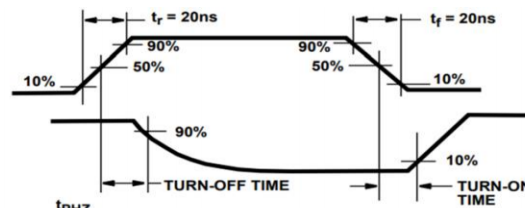
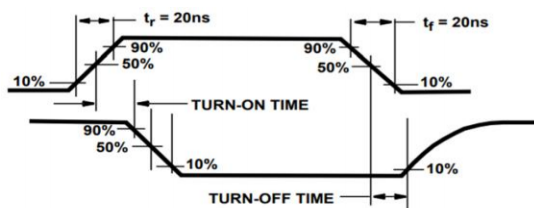
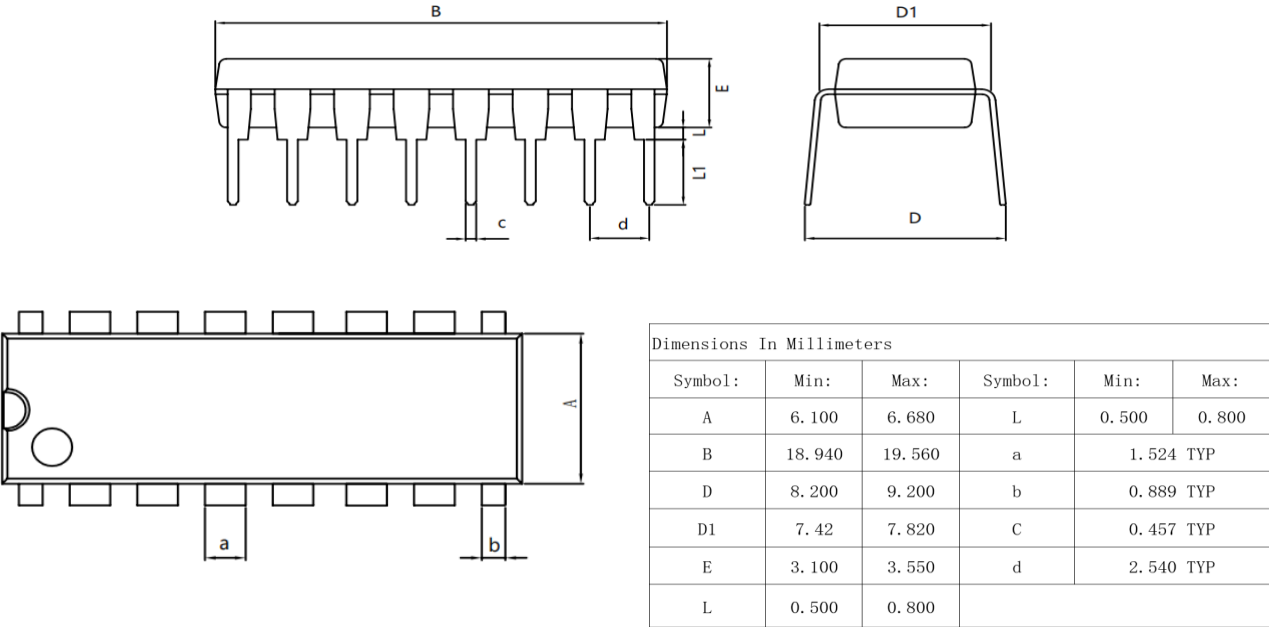


Fig. 10 同一通道信号串扰

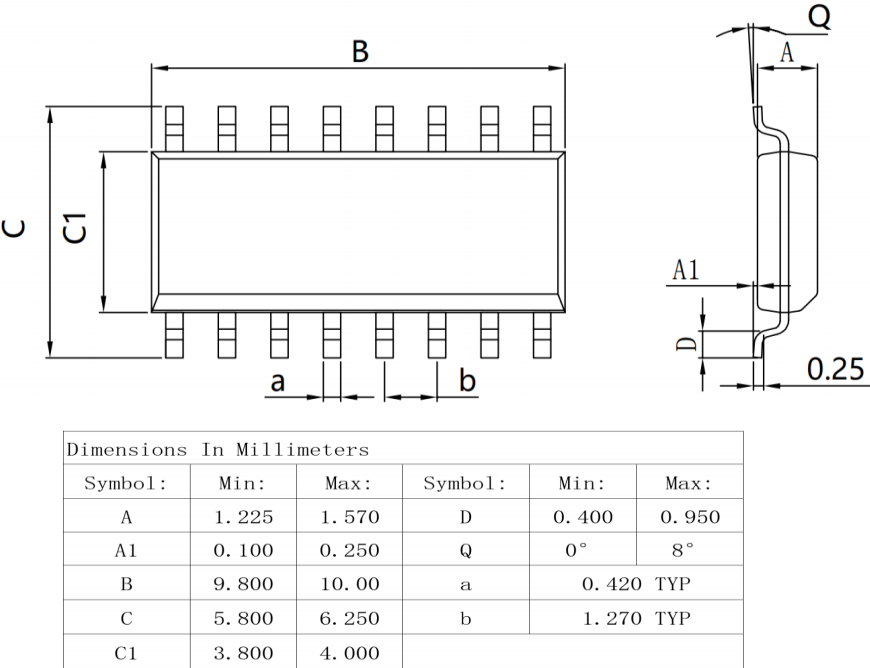
2、波形测量示意图



封装信息
DIP16



SOP16



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